DEPARTMENT OF ELECTRONICS & INSTRUMENTATION
ENGINEERING

Post-Graduate programme
M.Tech.(VLSI & EMBEDDED SYSTEMS)

Rules, Regulations, Scheme of Instruction & Evaluation and Syllabi

KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE::
WARANGAL-506015

KAKATIYA UNIVERSITY,WARANGAL
The course structure and scheme of Evaluation (Semester wise) for the
Post-Graduate programme
## M.TECH. (VLSI & EMBEDDED SYSTEMS)
### SEMESTER – I

<table>
<thead>
<tr>
<th>Course Number</th>
<th>Name of the Course</th>
<th>Periods per Week</th>
<th>Internal Examination</th>
<th>End Semester Examination</th>
<th>Total</th>
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### Elective-I
- 1.6.1 Micro Controller for Embedded Systems
- 1.6.2 Data Communication & Computer Networks
- 1.6.3 Digital Filter Design
- 1.6.4 Scripting Languages for VLSI Design Automation
KAKATIYA UNIVERSITY, WARANGAL

The course structure and scheme of Evaluation (Semester wise) for the Post-Graduate programme

M.TECH. (VLSI & EMBEDDED SYSTEMS)

SEMESTER – II

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<th>Name of the Course</th>
<th>Periods per Week</th>
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Elective – II

VLSI 2.6.1 – Digital Image Processing
VLSI 2.6.2 – CPLD & FPGA Architectures and Applications
VLSI 2.6.3 – Cellular and Mobile Communications

VLSI 2.6.4 – RF & Microwave Integrated Circuits
KAKATIYA UNIVERSITY, WARANGAL

The course structure and scheme of Evaluation (Semester wise) for the Post-Graduate programme

M.TECH. (VLSI & EMBEDDED SYSTEMS)

SEMESTER – III

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SEMESTER – IV

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VLSI 1.1  Optimization Techniques and Graph Theory

Semester: M.Tech. I semester  Lectures: 3 Periods
Duration of Univ. Exam: 3 Hours  Max Marks: 100 Marks
Max Marks: 100 Marks  Sessionals: 50 Marks

UNIT - I

Linear Programming:
Introduction, The simplex method, Artificial variable techniques, Duality in linear Programming, Dual simplex method, Integer linear programming, Gomory’s cutting plane method.

UNIT - II

Nonlinear Programming:

UNIT - III

Introduction to Graph Theory:
Basic definitions, results and examples relating to Graph Theory, Matrix representations of graphs, Isomorphic graphs, Definition of strongly, weakly, unilaterally connected graphs and deadlocks. Trees, spanning trees and Directed graphs.

UNIT - IV

Euler Graphs and Hamiltonian Graphs, Standard theorems, Planar Graphs, Euler’s formula, The Dual of a graph, Vertex coloring of a planar graph, Chromatic number Algorithm, The Four color problem.

Text Books:

VLSI 1.2  Digital Design
Semester: **M.Tech. I semester**  
Duration of Univ. Exam: **3 Hours**  
Lectures: **3 Periods**  
Max Marks: **100 Marks**  
Sessionals: **50 Marks**

**UNIT - I**

**Building Blocks for Digital Design:**  
Multiplexers, Demultiplexers, Decoders, Encoders, Comparators, Adders, ALU, Carry-Look-Ahead adder.

**Building Blocks with Memory:**  
Clocked building blocks, register-building blocks, RAM, ROM, PLA, PAL, Timing devices.

**UNIT - II**

**Design Methods:**  
Elements of design style, top-down Machines, ASM Chart notations.

**Realizing ASMS:**  
Traditional synthesis from ASM chart, multiplexer controller method, on-shot method, ROM based method.

**Design Case Studies:**  
Single pulsar, system clock, serial to parallel data conversion, traffic light controller.

**UNIT - III**

**Hierarchial Modelling Concepts:**  
Design methodologies, Modules, Module instances, parts of a simulation, Design and stimulus blocks Gate level, data flow, behavioural, modeling techniques, switch level modeling, PLI, delays.

**UNIT - IV**

**Fpga Architecture:**  
Channel-type FPGA’s – Xilinx, Actel, Structured Programmable array logic, Altera Computational Logic Arays – Algotronix, VLSI Primitives, Benchmarking.

**Design Process Flow:**  
Design capture, validation, Physical design, Placement and routing and wireability.

**Text Books:**

4. Samir Palnitkar,”Verilog HDL”, Pearson Education Asia, New Delhi, 2001
**VLSI 1.3  Analog Design**

**Semester:** M.Tech. I semester  
**Lectures:** 3 Periods  
**Duration of Univ. Exam:** 3 Hours  
**Max Marks:** 100 Marks  
**Sessionals:** 50 Marks

**UNIT - I**  

**UNIT - II**  
Differential amplifiers—single ended and Differential operation, Basic Differential pair, common mode response and Differential pairs with MOS loads. Operational amplifiers—General considerations, one stage OPAMPS, two stage OPAMPS. Gain Boosting, comparison, common mode feedback, Input range limitations, slew rate and power supply rejections.

**UNIT - III**  
Two stage MOS OP-AMP with cascodes. MOS Telescopic cascode OPAMP. MOS Folded cascode OP-AMP. Current feedback OPAMPS. Stability and frequency compensation of OPAMPS, Gain margin and Phase margin OPAMPS.

**UNIT - IV**  

**Text Books:**

**Reference Books:**
VLSI 1.4    VLSI Technology

Semester: M.Tech. I semester    Lectures: 3 Periods
Duration of Univ. Exam: 3 Hours    Max Marks: 100 Marks

Sessionals: 50 Marks

UNIT - I
Crystal structure, crystal growth and vapour phase epitaxy. Unit processes for VLSI-Oxidation, Photolithography, diffusion and ion implantation.

UNIT - II
Deposition of metal and dielectric films by vacuum evaporation, sputtering and CVD techniques, Wet chemical and Dry etching techniques.

UNIT - III

UNIT - IV
MOS based silicon ICs-NMOS ICs, Memory Devices, SOI Devices, BJT based ICs- choice of transistor types, advanced structures, Bipolar – CMOS (BICMOS) ICs. GaAs Technology: Ultra fast systems, Gas crystal structure, GaAs devices, GaAs fabrication, Comparison with other technologies.

Text Books:

Reference Books:
VLSI 1.5 Embedded System Concepts

Semester: M.Tech. I semester
Lectures: 3 Periods
Duration of Univ. Exam: 3 Hours
Max Marks: 100 Marks
Sessionals: 50 Marks

UNIT - I

Introduction to Embedded Systems:

Processor and Memory Selection:
Different Types of Processor Technologies, Processor Selection for an Embedded System, Different Types of Memory Devices, Memory Selection for an Embedded System.

UNIT - II

Communication Interfacing:

Device Drivers and Interrupts Servicing Mechanism:
Different types of Interrupts, Interrupt Servicing Mechanism, Device Servicing using ISR, Device Drivers, Parallel Port and Serial Port Device Drivers and Device driver Programming

UNIT - III

Software Engineering Practices in the Embedded Software Development Process:

Embedded Software Programming:
Assembly Language, C, C++ and Java

Programming models for Single and Multiprocessor Systems:
DFG, CDFG FSM, Petrinets, SDFG, HSDF, APEG and MTG

UNIT - IV

Real Time Operating Systems:

Commercial Real-Time Operating Systems:
uCOS-II, RTLinux, LYNXOS, PSOS, QNX//Neutrino, VX Works

Text Books:

Reference Books:

VLSI 1.6.1 Micro Controllers for Embedded Systems

Semester: M.Tech. I semester
Duration of Univ. Exam: 3 Hours
Lectures: 3 Periods
Max Marks: 100 Marks
Sessionals: 50 Marks

UNIT - I

Introduction to Embedded Systems:
Review of Microprocessors and their Features. 8 & 16 Bit Micro Controller Families (of Intel 8051 & 8097; Motorola 68HC11; Micro Chip's PIC 16C6X & 16C7X) and Micro controller hardware. Brief ideas on Embedded RISC Processor Architectures –ARM7TDMI/ARM9TDMI/10TDMI (Advanced RISC Machines Limited’s) and Motorola 680HX Processor IP Cores, their Features for Embedded Applications.

UNIT - II

Micro Controller Interfacing:
Using 8051, 68HC11 & PIC-16C7X - External Memory Interfacing – Memory Management Unit, Instruction and data cache, memory controller. On Chip Counters, Timers, Serial I/O, Interrupts and their use.

Software Development:

UNIT - III

Programming:
Instruction sets and assembly language program concepts and programming the 8051, 68HC11, PIC-16C7X Micro controllers & ARM7TDMI Core.


UNIT – IV

Ethernet Protocol, SDMA, Channels and IDMA Simulation, CPM Interrupt Controller and CPM Timers, power controls, External BUS Interface system Development and Debugging.

Case Studies:
Design of Embedded Systems using the micro controllers - 8051/ARM7TDMI, for applications in the area of Communications, Automotives.

Text Books:

Reference Books:
7. Craig Hollabaugh, Embedded Linux, Hardware, Software and Interfacing, Pearson Education.
VLSI 1.6.2  Data Communications and Computer Networks

Semester: **M.Tech. I semester**
Duration of Univ. Exam: **3 Hours**

Lectures: **3 Periods**
Max Marks: **100 Marks**
Sessionals: **50 Marks**

UNIT - I

Introduction to Network components, switching technologies, topologies, transmission media, protocols & routing.

WAN, NAN, LAN. Queuing theory models and applications computer networks, Data communication concepts – asynchronous & synchronous transmission, error correction codes & detectors.

UNIT - II

Transmission Protocols:
STOP – START, BSC, SDLC, HDLC, Retransmission techniques. LAN – components, Topologies, Access techniques, IEEE 802 standards, switched and Fast Ethernet, FDDI & SONET.

UNIT - III


UNIT - IV


Text Books:


Reference Books:

VLSI 1.6.3  Digital Filter Design

Semester: M.Tech. I semester  Lectures: 3 Periods
Duration of Univ. Exam: 3 Hours  Max Marks: 100 Marks

Sessionals: 50 Marks

UNIT - I

Multirate Digital Signal Processing:

UNIT - II

Linear Prediction and Optimum Linear Filters:
Representation of a stationary random process. Rational power spectra-A. R, M.A & ARMA processes. Relationship between the filter parameters and Auto-correlation sequence. Forward and Backward linear prediction

UNIT - III


UNIT - IV


Text Books:

Reference Books

VLSI 1.6.4  Scripting Languages for VLSI Design Automation
UNIT - I
Overview of Scripting Languages-PERL, CGI, VB Script, Java Script.

UNIT - II
PERL:
Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables.

UNIT - III
Inter process Communication Threads, Compilation & Line Interfacing.

UNIT - IV
Debugger Internal & Externals Portable Functions. Extensive Exercises for Programming in PERL.

Other Languages:
Broad Details of CGI, VB Script, Java Script with Programming Examples.

Text Books:
2. Larry Wall, Tom Christiansen, John Orwant, “Programming PERL”.
VLSI 1.7 Seminar

Class: M.Tech I Semester
Practicals: 1 Period
Internal Examination: 100 Marks

Note: Each student has to give independent seminars on the topics covering the following:

1. A Seminar Topic covering the state-of-the-art technical topics relevant up to the second Semester theory subjects, which would supplement and complement the programme are to be assigned to each student.

Guidelines:

1. The Students of M.Tech. I semester are to register a relevant topic with in 4 weeks of commencement of semester class work and submit the same to the department.
2. Evaluation of seminar consists of two components namely Report (50 marks) and Presentation (50 marks)
   (a) Report: Students are required to submit a report on the chosen seminar topic as per the prescribed format and last date specified by the Departmental Post Graduate Review Committee (DPGRC)
   (b) Presentation: The students are required to deliver the seminar before the DPGRC as per the schedule notified by the department.

   DPGRC will decide the course of action on the students who fail to submit the report and present the seminar.
VLSI 1.8    Analog Design Laboratory

Class: M.Tech I Semester   Practical: 3 Periods
Duration of University Examination: 3 Hours University Examination: 50 Marks
Sessionals: 50 Marks

List of Experiments:

1. Common Source Amplifier
2. Cascode Amplifier
3. Simple MOS Current Mirror
4. Cascode Current Mirror
5. Wilson and Widlar Current Mirrors
6. Differential Amplifier (Single Stage)
7. Transfer Characteristics of CMOS Inverter
8. Transfer Characteristics of CMOS NAND & NOR Gates
9. Transmission Gates
10. OP-AMP
11. Comparator
12. Folded Cascode OP-AMP
13. Transfer Characteristics of BJT’s
14. Transfer Characteristics of MOSFET’s
15. Source Degenerated Current Mirrors
16. Bandgap Preference – Voltage Reference
17. Bandgap Preference – Current Reference
Class: M.Tech I Semester
Duration of University Examination: 3 Hours

Practicals: 3 Periods
University Examination: 50 Marks
Sessionals: 50 Marks

List of Experiments: (Using VHDL, VerLog)

1. Design all Gates (AND, OR, NOT, NAND, NOR, XOR, XNOR)
2. Design Multiplexus and Demultiplexus
3. Design Decoder and Encoder
4. Design Half Adder & Full Adder
5. Implement ALU
6. Design Flip Flops
7. Design Ripple Counter
8. Design Shift Registers
9. Design Magnitude Comparator
10. Implement Bit-wise, logical and reduction operators.
11. Design Finite State Machines
12. Design Sequence Detectors
VLSI 2.1 Mixed Signal Design

Semester: M.Tech. II semester  
Duration of Univ. Exam: 3 Hours  
Lectures: 3 Periods  
Max Marks: 100 Marks  
Sessionals: 50 Marks

UNIT - I

Building blocks for CMOS amplifiers, design of current mirrors, differential amplifiers, CMOS operational transconductance amplifiers, Design of single ended telescopic cascode, folded cascode and two – stage amplifiers.

UNIT - II

Noise analysis and modelling; Time domain analysis, Frequency domain analysis, Noise Models for circuit elements, Noise analysis.

Switched capacitor Circuits: - Basic Building blocks, Basic operation and analysis, First order filters, charge injection , Switched capacitor gain circuits, Correlated Double-Sampling Techniques, other Switched Capacitor circuits.

UNIT - III

Comparators: Performance characteristics, OP-AMP based comparators, BICMOS comparators, Bipolar Comparators.

Sample and hold circuits: - Performance requirements, MOS sample and hold basics, clock feed through problems, S/H using T/H gate. Design of sample hold circuits and comparators.

UNIT - IV

DATA converter fundamentals: Ideal D/A converter, Ideal A/D converters, Quantization noise , signed codes, performance limitations.

D/A Converters: - decoder based converter, binary – Scaled Converters, Themometer code converter, hybrid converters.


Phase Locked Loops: - Basic loop architecture, PLLs with charge pump phase comparators, characteristics of PLLs , Applications PLLs

Text Books:
1. R.Gregorian, Temes,“Analog MOS integrated circuits for Signal processing”.
2. R.Gregorian,“Introduction to CMOS opamps and comparators”.
5. B.Razavi,’Monolithic Phase-locked loops and clock recovery circuits”.
VLSI 2.2  VLSI Physical Design

Semester: M.Tech. II semester  
Duration of Univ. Exam: 3 Hours  
Lectures: 3 Periods  
Max Marks: 100 Marks  
Sessionals: 50 Marks

UNIT - I
Scope of physical design – Components of VLSI – Various layers of VLSI – Typical structures of BJTS, MOSFETS, Resistors, capacitors, inductors, interconnects, brief review of technology, cost and performance analysis.

UNIT - II
Basic concepts of Physical Design - layout of basic structures – wells, FET, BJT, resistors, capacitors, contacts, vias and wires (Interconnects). Parasitics – latch up and its prevention, cell concepts. 
Design rules – fabrication errors – scalable design rules. Scalable CMOS (SCMOS) design rules, layout design, and stick diagrams, Hierarchical stick diagrams.

UNIT - III
Cell concepts – cell based layout design – wein berger image array – physical design of logic gates – NOT, NAND and NOR – design hierarchies. System level physical design, large scale physical design, interconnect delay modeling, floor planning, routing, clock distribution.

UNIT - IV
CAD Tools: 
Layout editors, Design rule checkers, circuit extractors – Hierarchical circuit extractors – Automatic layout tools, silicon compilers, modeling and extraction of circuit parameters from physical layout.

Text Books:

Reference Books:
VLSI 2.3  Embedded System Design Modeling, Synthesis and Verification
Semester: M.Tech. II semester  Lectures: 3 Periods
Duration of Univ. Exam: 3 Hours  Max Marks: 100 Marks
Sessionals: 50 Marks

UNIT-I
System Level Design Methodologies: Bottom-up Methodology, Top-down Methodology, Meet-in-the-middle Methodology, Platform Methodology, FPGA Methodology, System-level Synthesis, Processor Synthesis

UNIT-II

UNIT-III
Hardware Synthesis: RTL Architecture, Input Models, Estimation and Optimization, Register Sharing, Functional Unit Sharing, Connection Sharing, Register Merging, Chaining and Multi-Cycling, Functional-Unit Pipelining, Data path Pipelining, Control and Data path Pipelining, Scheduling, Interface Synthesis

UNIT-IV
Verification: Simulation Based Methods, Formal Verification Methods, Comparative Analysis of Verification Methods, System Level Verification
A Unified Embedded Co-design Methodology using UML and SystemC
Refined design methodology, SystemC 2.0, UML 2.0 Diagrams, UML Profile for SystemC, Modeling and generating test cases for Transactional Level SystemC design

Text Book
1. Embedded System Design Modeling, Synthesis and Verification, Gajski, D.D; Abdi,S;Gerstlauer,A;Schirner,G;Springer publications, ISBN:978-1-4419-0503-1

Reference Book
VLSI 2.4  Low Power VLSI Design

Semester: **M.Tech. II semester**  
Duration of Univ. Exam: **3 Hours**  
Lectures: **3 Periods**  
Max Marks: **100 Marks**  
Sessionals: **50 Marks**

**UNIT - I**

**UNIT – II**
Design styles and testing – low voltage CMOS circuit design styles, leakage current in deep submicron transitions and design issues, minimization of short channel effects (SCE) and hot carrier effects. Testing of deep sub micron ICs with elevated intrinsic leakage.

**UNIT - III**
Low power architectures – MOS static RAM cells, banked organization SRAMS, reducing voltage swing on bit lines, write lines, driver circuits and sense amplifier circuits. Energy computing and recovery techniques – energy dissipation using an RC model, energy recovery circuit design, design with partially reversible logic and supply clock generation.

**UNIT - IV**
Software design for low power - dedicated hardware Vs software implementation, power dissipation, estimation and optimization. Automated power code generation and co design for low power.

**Text Books:**
VLSI 2.5  Design for Testability

Semester: **M.Tech. II semester**  
Lectures: **3 Periods**  
Duration of Univ. Exam: **3 Hours**  
Max Marks: **100 Marks**  
Sessionals: **50 Marks**

UNIT - I  
Introduction to Test and Design fro Testability (DFT) Fundamentals.

**Modeling:**  

UNIT - II  
Testing for single stuck faults (SSF) – Automated test pattern generation (ATPG/ATG) for SSFs in combinational and sequential circuits, Functional testing with specific fault models. Vector simulation – ATPG vectors, formats, Compaction and compression, Selecting ATPG Tool.

UNIT - III  
Design for testability – testability trade-offs, techniques. Scan architectures and testing – controllability and absorbability, generic boundary scan, full integrated scan, storage cells for scan design. Board level and system level DFT approaches. Boundary scan standards. Compression techniques – different techniques, syndrome test and signature analysis.

UNIT - IV  
Built-in self-test (BIST) – BIST Concepts and test pattern generation. Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO. Brief ideas on some advanced BIST concepts and design for self-test at board level.

Memory BIST (MBIST):  
Memory test architectures and techniques – Introduction to memory test, Types of memories and integration, Embedded memory testing model. Memory test requirements for MBIST. Brief ideas on embedded core testing.

Text Books:  
VLSI 2.6.1  Digital Image Processing

Semester: M.Tech. II semester  Lectures: 3 Periods
Duration of Univ. Exam: 3 Hours  Max Marks: 100 Marks
Sessionals: 50 Marks

UNIT - I
Introduction:

Digital Image Fundamentals:
Elements of Visual Perception, Image Sensing and Acquisition, Image Sampling and Quantization, Basic Relationships between Pixels

UNIT - II
Image Enhancement in the Spatial Domain:
Some Basic Gray Level Transformations, Histogram Processing, Enhancement Using Arithmetic/Logic Operations, Basics of Spatial Filters.

Image Enhancement Sharpening Spatial Filters. Domain in the Frequency:
An Introduction to the Fourier Transform and the Frequency Domain, Smoothing Frequency Domain Filters, Sharpening Frequency Domain Filters, Implementation.

UNIT - III
Image Restoration:
Noise Models, Restoration in the Presence of Noise Only-Spatial Filtering, Periodic Noise Reduction by Frequency Domain Filtering, Linear Position - Invariant Degradations Estimating the degradation Function, Inverse Filtering, Minimum Mean square Error filtering, Geometric Mean Filter and Transformations.

Image Compression:

UNIT - IV
Image Segmentation:
Detection of Discontinuities, Edge Linking and Boundary Detection, Thresholding, Region Based Segmentation, Segmentation by Morphological Watersheds, The Use of Motion in Segmentation.

Representation and Description:
Representation, Boundary Descriptions, Regional descriptors.

Text Books:

VLSI 2.6.2  CPLD and FPGA Architectures and Applications
Semester: M.Tech. II semester  
Lectures: 3 Periods  
Duration of Univ. Exam: 3 Hours  
Max Marks: 100 Marks  
Sessionals: 50 Marks

UNIT - I

Programmable Logic:
Read Only Memory (ROM), Programmable Logic Array (PLA)/Programmable Array Logic (PAL). Sequential Programmable Logic Devices (PLDs). Programmable Gate Arrays (PGAs) – Features, Programming and applications using Complex Programmable Logic Devices (CPLDs) - Altera series – Max 5000/7000 Series and ALTERA FLEX Logic – 10000 Series CPLDs. AMD’s – CPLD (Mach 1 to 5); Cypress FLASH 370 Device Technology, Lattice pLSI’s Architectures – 3000 Series – Speed Performance and in system programmability.

FPGAs:
Field Programmable Gate Arrays – Logic blocks, routing architecture, Design flow, Technology Mapping for FPGAs, Case studies – Xilinx XC4000 & ALTERA’s FLEX 8000/10000 FPGAs: AT & T – ORCA’s (Optimized Reconfigurable Cell Array): ACTEL’s – ACT 1, 2, 3 and their speed performance.

UNIT - II

Finite State Machines (FSM):

UNIT - III

FSM Architectures and Systems Level Design:

UNIT - IV
Digital Front End Digital Design Tools for FPGAs & ASICs:
Using Mentor Graphics EDA Tool (“FPGA Advantage”) - Design Flow Using FPGAs -
Guidelines and Case Studies of parallel adder cell, parallel adder sequential circuits, counters,
multiplexers, parallel controllers.

Text Books:
   Hall, 1994.
2. S. Trimberger, “Field Programmable Gate Array Technology”, Kluwer Academic
3. J. Old Field, R. Dorf, “Field Programmable Gate Arrays”, John Wiley and Sons,

Reference Books:
2. PLD & FPGAs from Xilinx, Altera, AMD.
VLSI 2.6.3 Cellular and Mobile Communications

Semester: M.Tech. II semester
Duration of Univ. Exam: 3 Hours
Lectures: 3 Periods
Max Marks: 100 Marks
Sessionals: 50 Marks

UNIT - I

Introduction to Cellular Mobile Systems:
Operation performance and planning of cellular-analog and digital systems. System design-concepts of frequency reuse, Co-channel interference reduction, Hand-off mechanism, Cell splitting & Components of cellular system.

UNIT - II

Co-channel Interference, Real time interference & reduction, Power measurement at mobile receiver and service area calculations, and interference between systems. Frequency management: Spectrum utilization, channel, co-channel assignment and call blocking algorithms.

UNIT - III

Hand-off and dropped calls queuing and introduction to dropped cell rate. Review of digital communication techniques-ARQ techniques, Digital speech & multiple access schemes for mobile telephonic.

UNIT - IV

Digital Cellular Systems:
Important concepts of - GSM, TDMA, CDMA, PDC, DECT, CDPD, PCN and PCS Systems. CDMA cellular radio networks, brief ideas on intelligent networks for wireless communication - AIN, SS7, ISDN, FPLMTS and ATM Networks.

Text Books:

Reference Books
VLSI 2.6.4  RF and Microwave Integrated Circuits

Semester: M.Tech. II semester  Lectures: 3 Periods
Duration of Univ. Exam: 3 Hours  Max Marks: 100 Marks
Sessionals: 50 Marks

UNIT - I
Analysis and design of RF and microwave lines – Review of transmission lines, parallel plate transmission line, low frequency solution, high frequency solution, strip line and micro strip transmission lines, low frequency solution, high frequency properties of microslot line, co planer wave guides, coupled microstrip lines, spiral inductors – capacitors.

UNIT - II
Microstrip / Stripline based filters. Resonators, phase shifters, micro strip based gyrators, circulators and isolators, directional couplers.

UNIT - III
Microwave active devices – microwave transistors, Gaas FETS (Structures, equivalent circuit), Low noise amplifiers, power amplifiers, oscillators, detectors, mixers, modulators and switches.

UNIT - IV
Technology of MICS: Deposition techniques – vacuum evaporation – Vacuum sputtering ion plating, MBE (Molecular Beam Epitaxy) – photo lithography, mask preparation, thick film technology, GaAs technology. MIC Packaging: Component attachment, bonding techniques, solder reflow techniques, input/output terminations, testing.

Text Books:

Reference Books:
VLSI 2.7  Physical Design Automation Laboratory

Class : M.Tech II Semester  Practical : 3 Periods
Duration of University Examination: 3 Hours University Examination : 50 Marks
Sessionals: 50 Marks

List of Experiments:

1. Layout of Basic Devices
2. Partitioning Algorithms
3. Place and Route Algorithms
4. Floor Planning and Pin Assignment
5. Routing
6. Clock distribution
7. Interconnect Delay modeling
9. Automatic layout tools
10. Silicon Compilers.
11. Design rule checkers.
List of Experiments:

1. Design All Basic Logic Gates Using SystemC
2. Design Finite State Machines and Sequence Detector Using SystemC
3. Simple Bus Model using SystemC
4. System level Modeling and Design using UML 2.0 Profile
   i. Composite Structure Diagrams
   ii. Interaction Overview Diagrams
   iii. Sequence Diagrams
   iv. State hart Diagrams
   v. Timing Diagrams
   vi. Class Diagrams
   vii. Code Generation from Class Diagrams and State hart Diagrams
5. Implementing IPC Mechanisms using SystemC
6. Serial Communication Programming
7. Writing Device Drivers
8. RTOS Programming
VLSI 3.1 Industrial Training

Class: M.Tech III Semester

Guidelines for Industrial Training:

1. M.Tech. Coordinator in consultation with the Training & Placement section has to procure training-cum-dissertation slots, for the students before the last day of instruction of II semester.

2. The students are to confirm their training slot by the last day of II semester.

3. The students after 8 weeks of Industrial Training shall submit a certificate, and the last date specified and a report in prescribed format by the DPGRC.

The DPGRC will decide the course of action on the students who fail to submit the training certificate and report.
VLSI 3.1 Industrial Training

Class: M.Tech III Semester

**Guidelines for Industrial Training:**

4. M.Tech. Coordinator in consultation with the Training & Placement section has to procure training-cum-dissertation slots, for the students before the last day of instruction of II semester.

5. The students are to confirm their training slot by the last day of II semester.

6. The students after 8 weeks of Industrial Training shall submit a certificate, and the last date specified and a report in prescribed format by the DPGRC.

The DPGRC will decide the course of action on the students who fail to submit the training certificate and report.
Class: M.Tech IV Semester

Guidelines for Dissertation:

The Department Post-Graduate Review committee is to be constituted with 5 members i.e. Chairman – Head of the Department, Convenor – M.Tech. Coordinator and 3 other faculty members including supervisor.

The committee is to evaluate the progress of the Dissertation conducting 2 presentations in third semester and monthly presentations in fourth semester.

III – Semester Total Marks – 100

50 marks for presentations
50 marks for regular evaluation by supervisor.

1st presentation (Registration Seminar) after 6 weeks from the commencement of the semester for 25 marks
2nd presentation (Progress Seminar) after 12 weeks from the commencement of the semester for 25 marks

Registration Seminar: Project proposal (problem specification, expected outcome)

IV – Semester Total Marks – 200

Progress Seminar: Status of the dissertation – work already carried out, balance of work to be carried out – Progress seminars are to be carried out every month between 1st and 5th.

Synopsis Seminar: Together with synopsis a presentation to be made and the dissertation should be demonstrated two weeks before the submission date.

Supervisors are to evaluate the Dissertation regularly, based on the progress report submitted by the students in every week and the same should be recorded.

Project work will be carried out in III and IV semesters under the supervision of a faculty member from within the respective department. Students may be permitted to work under the joint guidance of two members of the faculty – in which case, one of the guides may be from an allied department.

A student may, however, be permitted by the Head of the Department concerned to work on a project in an Industrial / Research organization, in the project semesters. In
such case, the faculty guiding the student shall be called the internal guide and the scientist / manager guiding, the student (at site) shall be called the external guide.

No student will be allowed to submit the project report before 48 weeks and after 52 weeks from commencement of III semester.

The DPGRC will decide the course of action on the students who fail to submit the dissertation.