## SCHEME OF INSTRUCTION AND EVALUATION

I SEMESTER OF II YEAR OF 4-YEAR B.TECH. DEGREE PROGRAMME

ELECTRONICS & COMMUNICATION ENGINEERING

<table>
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<tr>
<th>Course Number</th>
<th>Course</th>
<th>Hours of Instruction per week</th>
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<td>Mathematics – II</td>
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<td>EI 213</td>
<td>Electronic Measurements &amp; Instrumentation</td>
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<td>Switching Theory &amp; Logic Design</td>
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<td>EE 216</td>
<td>Electrical Technology</td>
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(6+2) Total: 30 Hours
MH 211 MATHEMATICS – II

Class: B.Tech. II/IV, I-Semester
Branch: CSE, IT, Mech, Civil, ECE, EEE, E&I
Duration of Univ. Examination: 3 Hrs.

Lectures: 3 Hrs, Tutorials: 1
Univ. Examination: 100 marks
Sessionals: 50 marks

UNIT – I

UNIT – II

UNIT – III

UNIT – IV
PARTIAL DIFFERENTIAL EQUATIONS: solution of wave equation, Heat equation and Laplace equation by the method of separation of variables and their application in problems of vibrating string, one dimensional unsteady heat flow and two dimensional steady heat flow (Problem based on Fourier – Trigonometric series only).

TEXT BOOKS:

REFERENCE BOOKS:
UNIT-I


BRIDGES: Wheatstone Bridge, Kelvins Double Bridge, Maxwell’s Bridge, Schering bridge and Wien’s Bridge. (9+3)

UNIT-II


SIGNAL ANALYSIS INSTRUMENTS: Frequency Selective & Meterodyne Wave Spectrum Analyzers – Harmonic distortion Analyzers, Total Harmonic distortion – Elementary Magnetic tape Recorder. (9+3)

UNIT – III

TRANSDUCERS: Transducer and its classification, Ideal Requirements of Transducer – Resistive Transducers: Potentiometric type, Strain Gauge type (Gauge factor derivation, SG materials, Bonded and unbounded strain gauges) – Capacitive Transducers : Variable gap type, variable area type & variable Dielectric type – Inductive Transducers: Variable Reluctance type, LVDT type – Piezo Electric Transducers (Piezoelectric effect, Piezoelectric materials, Frequency Response of PZT) – Phot electric Transducers (LDR, Photo transistor, Photo Voltaic Cell). (9+3)

UNIT – IV


Text Books:


Reference Books:

UNIT – I

Number Systems and Codes: Review of Number systems, binary arithmetic – binary weighted and non weighted codes – error detecting and error correcting codes.


UNIT – II

Design of Combinational Circuits:


UNIT – III

Sequential Circuits: Flip Flops – SR flip flop, JK flip flop, D flip flop, T flip flop, Excitation tables- Race around condition, Master slave flip flop, Excitation tables.

Design of Synchronous and Asynchronous counters, shift registers - Modes of operation, Bidirectional shift registers, Ring counters, Johnson counters. Glitches and delay problems in counters.

UNIT – IV

Synchronous Sequential Circuits and Iterative Networks: State table, state diagram, state assignment, state minimization, synthesis of synchronous, sequential circuits – Sequence detectors – Binary counters.

Capabilities and Minimization of Sequential Machines: Mealy and Moore Machines – Capabilities and limitations of finite state machine – state equivalence and machine minimization.

TEXT BOOKS:

REFERENCE BOOKS:
EI 215 ELECTRONIC DEVICES AND CIRCUITS – I

Class: II/IV B.Tech. I - Semester Lectures: 3, Tutorial: 1
Branch: ECE, E&I, EEE University Examination: 100 marks
Duration of University Examination: 3 Hours Sessionals: 50 marks

UNIT – I

UNIT – II
Transistors, current components in NPN and PNP transistors, Ebers-Moll model. Small Signal LF h-parameter model, Determination of h-parameters – Analysis of transistor amplifier using h-parameters in CE, CB and CC configuration – simplified analysis for these configurations. BJT as switch

UNIT – III

UNIT – IV

TEXT BOOKS:

UNIT – I
Ohm’s Law, Network Elements, Kirchhoff’s Laws, Source Transformation, Mesh and Nodal Analysis, Power in Electric Circuits, Series, Parallel and Series Parallel and Combination of Resistances, network reduction by Star – Delta Transformation, Superposition, Thevenin’s Norton’s, and Maximum Power transfer theorems. (9+3)

UNIT – II
1 – Phase A.C. Circuits: Phasor representation of sinusoidal quantities, Average, R.M.S. values and Form factor, A.C. through Resistor, Inductor and Capacitor, Analysis of R-L-C series and parallel circuits, Power factor, power triangle, Series Resonance.
3-ϕ A.C. Circuits: Production of 3-ϕ Voltages, Voltage & Current relationships of Line and Phase values for Star and Delta Connections, 3-ϕ Power Measurement by two-wattmeter method for balanced loads. (9+3)

UNIT – III
Magnetic circuits: Self and Mutual Inductance, Dot Convention, Coefficient of Coupling. B-4 loop curve.

UNIT – IV
1-ϕ Induction Motors: Production of Rotating Field in various type of 1-phase motors split phase, capacitor start, capacitor run, shaded pole motors and applications.
Synchronous Generators and Motors: Principal of Operation and its Applications. (9+3)

TEXT BOOKS:
1. Vincent Del Toro “PRINCIPLES OF ELECTRICAL ENGINEERING” PHI.
2. Edward Hughes, “ELECTRICAL TECHNOLOGY”, Pearson Publisher.

REFERENCE BOOKS:
1. M.S. Naidu & S.Kamakshaiah, “INTRODUCTION TO ELECTRICAL ENGINEERING.
2. B.L. Thereja, “ELECTRICAL TECHNOLOGY” S.Chand & Company Ltd.
3. Sudhakar and Shyam Mohan “ NETWORK ANALYSIS AND SYNTHESIS” TMH.
4. Nagrath and Kothari “ BASIC ELECTRICAL ENGINEERING” TMH.
UNIT – I


**Time response analysis of Networks:** Transient analysis of R-L, R-C, R-L-C series & parallel networks with step, impulse, sinusoidal and pulse excitation – Initial conditions – Special signal wave form Ramp, Triangular train of pulses, delayed input.

**P-SPICE:** Introduction to P-SPICE representation of circuit elements – Analysis of Circuits using P-SPICE – Simple problems.

UNIT – II


UNIT – III

Network Functions: Network function for 1-port and 2-port networks and their relationships – Ladder Networks – General Networks – Poles and zeros of Network functions – Restrictions of pole zero locations for driving point functions.

**Network Synthesis:** Positive real function properties – Hurwitz Polynomials – Even and odd functions – Test for positive Real functions – Elementary synthesis operation – properties and Foster and Cauer forms of RL, RC and LC networks. (9+3)

UNIT-IV

Image and iterative impedance, transfer constants, insersion loss, attenuators, Passive Filters: LPF, HPF, BPF and BRF constant K-and m derived filters, composite filters.

**TEXT BOOKS:**
1. M.E.Van Valkenberg “ Network Analysis” PHI.

**REFERENCES:**
1. J.Edminister & M.Nahvi. “ Electric Circuits” Schaum’s outlines, TMH.
2. D.Roy Choudhary “Networks analysis and Synthesis” New Age Publishers
LIST OF EXPERIMENTS

1. Verification of Kirchhoff’s Laws
2. Verification of Superposition Theorem.
3. Verification of Thevenin’s Theorem.
4. Voltage and Current relationships of line and phase values in star, delta connections and 3-phase power measurement by two-wattmeter method.
5. Frequency response of R-L-C series circuit
6. Determination of Parameters of choke coil.
7. S.C. Tests on 1-phase transformer to determine the equivalent circuit parameters and predetermination of efficiency.
8. Efficiency and voltage Regulation of a 1-phase transformer by direct load test.
9. Speed control and Swinburne’s test on D.C. shunt motor to predetermine efficiency as Motor and Generator
11. Load test on D.C. shunt Generator
12. Demonstration Experiments
   a) D.C. Motor
   b) D.C. Generator (O.C.C.)
   c) 1-phase Induction Motors
   d) Alternators.
EI 2110 ELECTRONIC DEVICES & CIRCUITS-I LAB

Class: II/IV B.Tech. I Semester
Branch : E&I, ECE

Practicals : 2 Hrs
University Examination: 50 Marks
Sessionals : 25 Marks

Duration of University Examination: 2 Hrs

LIST OF EXPERIMENTS

2. Half-wave / Full – wave Rectifier with and without filters
3. Voltage Regulator
5. FET Static Characteristics CS (Common Source
6. Biasing Circuits (BJT) fixed bias, collector to base bias, self-bias
7. Transistor as Switch.
8. SCR characteristics.
9. UJT characteristics.
10. LED / Photodiode / Photo transistor characteristics.
## SCHEME OF INSTRUCTION AND EVALUATION
### II SEMESTER OF II YEAR OF 4-YEAR B.TECH. DEGREE PROGRAMME

### ELECTRONICS & COMMUNICATION ENGINEERING

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(6+2) Total : 30 Hours
MH 221 MATHEMATICS – III

Class: B.Tech. II/IV, II-Semester lectures: 3 Hrs, Tutorials: 3 Hrs.
Branch: CSE, IT, Mech, Civil, ECE, EEE, E&I Univ. Examination : 100 Marks
Duration of Univ. Examination: 3 Hrs. Sessionals: 50 marks

UNIT – I
MATRICES: Rank of a matrix – Solution of System of Linear equations – Linear dependence and independence of vector – Characteristics roots and Characteristics vectors of a matrix–Cayley Hamilton Theorem (without proof) – Reduction to diagonal form and normal form. Reduction of a quadratic form to canonical form. (8+3)

UNIT – III

UNIT – III
NUMERICAL DIFFERENTIATION AND INTEGRATION: First and second derivatives using forward and backward interpolation. Numerical Integration-Trapezoidal and Simpson’s rule. (8+3)

UNIT – IV
NUMERICAL SOLUTION OF ORDINARY DIFFERENTIAL EQUATIONS: Taylor’s methods, Euler’s method, Runge – Kutta methods of second and fourth orders. (8+3)

TEXT BOOK:

REFERENCE BOOKS:
1. S.S.Sastry, “Introductory Numeriical Analysis”.
UNIT - I

ELECTRO STATICS: Coulomb's law, Electric field intensity, Field due to line charge and sheet of charge, Flux density Gauss's law and its applications, Electric Potential, potential gradient, Relation between E & V, Poissons's and Laplace's equation. Energy density, Boundary conditions between two dielectrics, capacitance - parallel plate, co-axial, spherical cable.


UNIT - II


ELECTROMAGNETIC WAVES: Wave equations for free space and conducting medium, Uniform plane waves, Sinusoidal time varying fields, conductors and dielectric, wave propagation through good conductors and good dielectrics, Polarisation, Direction cosines, Reflection of EM waves by a perfect conductor, a perfect dielectric, surface impedance, skin effect.

UNIT – III

POYNTING VECTOR: Poynting theorem, Instantaneous, Average and complex poynting vectors, power loss in a plane conductor.

GUIDED WAVES & WAVE GUIDES: Waves between parallel planes, TE, TM, TEM Waves characteristics of TE, TM & TEM Waves. Rectangular wave guides, TE & TM waves in wave guides, Impossibility of TEM waves in rectangular wave guides, introduction to circular wave guides.

UNIT - IV

Transmission Lines : Primary & Secondary constants, Transmission Line equations, Phase and group velocities, loss less ness / Low Loss characterization, distortion and loading, expression for i/p impedance, SC & OC lines, UHF lines as circuit elements, λ/8, λ/4, λ/2, lines – impedance transformations, smith chart – its configuration and
applications, single and double stub matching techniques. Illustrative problems (Incl, of
smith chart applications and single stub matching) (9+3)

**TEXT BOOKS:**

1. “ELECTRO MAGNETIC WAVES AND RADIATING SYSTEMS .”
   - E.C. Jordan & K.G. Balman, Prentice Hall of India

2. “TRANSMISSION LINES AND NETWORKS” – By Umesh Sinha, .Satya
   Prakashan (Tech. India Publication) New Delhi.


**REFERENCE BOOKS:**

1. Elements of Electromagnetics – by Mathew N.O. Sadiku, Oxford Univ Prem, 2/e.
EC 223 DIGITAL INTEGRATED CIRCUITS

Class: II/IV B.Tech. II Semester. Lectures:3, Tutorials:1
Branch: ECE University Examination: 100 marks
Duration of University Examination: 3 hours Sessionals: 50 marks

UNIT-I

Logic Families: Detailed study of RTL, I^2L, DCTL, DTL, HTL, TTL, ECL, MOS & CMOS families and their properties and comparison.

UNIT-II

Programmable Logic Devices: PLAs, PALs, FPGAs, CPLDs.
Algorithmic State machines: ASM charts, ASM blocks, timing considerations, data path design, control logic design, design with MUXs and Flip flops, typical examples.

UNIT-III

EDA Tools: Introduction of HDL Simulation & Synthesis, VHDL – Basic Language elements and various modellings.


UNIT-IV

DATA FLOW Modeling: Cuncurrent Vs sequential Signal assignment, multiple drivers, signal assignment statements, block statement simple programming.
Structural modeling: Component declaration, component instantiation, simple programming.
Generics and Configurations.

Text Books:

1. Digital Integrated Electronics: Tanb & Schiling –
2. Digital Design – M.Moris Mano – PHI.
3. VHDL Primer – J. Bhaskar – PHI.

References Books:

UNIT-I
SMALL SIGNAL LOW FREQUENCY TRANSISTOR AMPLIFIER CIRCUITS:
Analysis of Single Stage transistor amplifier circuits using $h$-parameters, RC coupled amplifier – Frequency response analysis, cascaded amplifiers.

HIGH FREQUENCY TRANSISTOR AMPLIFIER CIRCUITS:
High frequency model of a transistor $\alpha$ and $\beta$ cut-off frequencies, single Stage and Multistage amplifiers at High frequencies Calculation of Band Width of single and multistage amplifiers.

UNIT-II
DC AMPLIFIERS:
DC amplifiers, drift compensation techniques, differential amplifiers.
FET AMPLIFIERS:
FET Low frequency and High Frequency models; Low and High frequency response of amplifier circuits, Analysis of Single and Multistage amplifier circuits.

UNIT-III
FEED BACK AMPLIFIERS:
Concept of feedback, Classification of feedback amplifiers, general characteristics of negative feedback amplifiers, effect of feedback on amplifier characteristics.
OSCILLATORS:
Condition for Oscillations, RC and LC type oscillators, crystal oscillators, frequency and amplitude stability of Oscillations.

UNIT-IV
POWER AMPLIFIERS:
Class A,B and AB power amplifiers: Push-Pull and Complementary push-pull amplifiers, design of heat sinks, power o/p efficiency, cross – over and Harmonic Distortion.
TUNED AMPLIFIERS:
Single tuned and Double tuned voltage amplifiers, Inter stage design, stability considerations, class B and Class C tuned Power amplifiers.

TEXT BOOKS:

REFERENCE BOOKS:
EC 225 SIGNALS & SYSTEMS

Class: II/IV B.Tech. II Semester. Lectures:3, Tutorials: 1
Branch: ECE, EIE, EEE University Examination: 100 marks
Duration of University Examination: 3 hours Sessionals: 50 marks

UNIT-I

**Signals** – Signals and their representation, classification of signals, singularity functions – Impulse, step, ramp functions, representation of signals with singularity functions, exponential functions.
System: Definition, Classification of Systems, Convolution integral, graphical convolution.

**Signal Approximation** – Approximation of a function by a set of mutually orthogonal functions, mean square error, complete set of orthogonal functions orthogonality in complex functions, Trigonometric and exponential Fourier series, representation of periodic functions by Fourier series, complex Fourier spectrum.

UNIT-II

**Fourier Transforms and their applications to systems** – Fourier transform definition, properties of F.Ts, energy spectral density, parsevals theorem, power spectral density, Hilbert transforms and properties.

**Linear Systems** – impulse response, response of a linear system, linear time invariant system, linear time variant system, transfer function of LTI system.

UNIT-III

**Random Variables & Processes** – Probability, Joint Probability, Statistical independence, Random Variables, cumulative distribution function, probability density function, relation between probability & probability density, joint commutative distribution, average value of random variables, variance of a random variable, tchebycheff's inequality, the Gaussian probability density, the error function, Rayleigh probability density, mean & variance of the sum of random variables, correlation between random variables, central limit theorem.

UNIT-IV

**Discrete Time Signals & Systems**: Discrete time signals, representation, operations on sequences, Discrete time systems and classification, LTI systems, Linear Convolution, Difference equations.

**Z-Transforms**: ROC, properties of Z-Transforms Inverse Z-Transforms, Causality and stability.


**TEXT BOOKS:**
2. Zeimer, Signals & Systems, PHI.

**REFERENCE BOOKS:**
1. Oppenheim, Willsky & Young; Signals and Systems PHI, EEE, New Delhi.
3. B.P. Lathi, Signals & Systems and Communication – BSP.
CS 2210 PROGRAMMING AND DATA STRUCTURES

Course: II/IV B.Tech. II Semester  
Theory: 3 Periods/week
Branch: ECE  
Tutorial: 1 Period/week
External Examination: 3 Hours  
External Evaluation: 100
Internal Examination: 2 Hours  
Internal Evaluation: 50

UNIT-I  
Basics of Data Structures: Data structure definition, Applications of data structures, Algorithms, Programs, Design and analysis steps, Time and Storage analysis.
Arrays: Representation of arrays, Memory allocation for arrays, Operations on arrays, Applications of arrays, Pointer arrays, Sparse matrix Operations, Polynomial operations.
Stacks: Stack model and operations, Stack implementation, Multiple stacks.
Stack applications: Infix, Prefix, Postfix notations, Conversion and evaluation of expressions, Recursion.

UNIT-II  
Queues: Queue model and operations, Queue implementation, Circular queue, Circular queue implementation, Dequeues, Priority queues, Applications of queues.
Linked Lists: Definition, Representation of a linked list in memory, Operations on single linked list, Double linked list, Operations on double linked list, Circular Linked list, Linked list operations with header node, Implementation of stacks and queues using linked lists.
Applications of linked lists: Polynomial representation, Polynomial operations, Dynamic storage Management, Generalized lists, Garbage collection and Memory compaction.

UNIT-III  
Trees: Basic terminologies, Binary trees representation using arrays, Binary tree representation using linked lists, Binary tree traversal algorithms: inorder traversal, preorder traversal, postorder traversal, Binary search tree, Binary search tree operations(addition of a node, deleting a node)
Graphs: Terminology, Graph representation methods: adjacency matrix, adjacency lists, adjacency multilists, Graph traversal algorithms: Depth first search, Breadth first search, spanning trees, Minimum spanning tree, Shortest paths.

UNIT-IV  
Searching: Linear search algorithm, Binary search algorithm, Fibonacci search algorithm, Comparison of search algorithms.
Sorting: Insertion sort algorithm, Shell sort algorithm, Quick sort algorithm, Merge sort algorithm, Two way merge sort algorithm, Heap sort algorithm.
(All above topics with intuitive notion of complexity of algorithms)
SUGGESTED TEXT / REFERENCE BOOKS:


LIST OF EXPERIMENTS

1. Logic gates: Aim: Realization of all logic gates using NAND / NOR gates and verification of their truth tables.
3. Half and Full subtractors: Aim: Realization of half and full subtractors using NAND gates and verification of their truth tables.
4. BCD Adder: Aim: Design of BCD Adder using 4 bit Full Adder (IC7483) and Logic gates and verification of its truth table.
5. “n” bit Ripple counter: Aim : Design of “n” bit ripple counter using JK/T FFS and verification of its function table.
7. 4 bit Ring and Johnson Counters: Aim: Design of 4 bit Ring and Johnson counters using DFFS (IC7474) and verification of their function tables.
8. Decade Counter and Decoders: Aim: Verification of the function table of Decade Counter (IC7490) and displaying its output in decimal form using decoders (IC7442-BCD to 7 segment and IC7446 – BCD to Decimal)
9. 4:1 MUX: Aim: Design of a 4 to 1 multiplexer using logic gates and verification of its function table.
10. 8:1 MUX : Aim: Realization of Boolean expressions using 8 to 1 MUX
11. 4 bit shift Register: Aim: Design of a 4 bit shift register and verification of its different modes of operation.
12. Transfer Characteristic of NAND gate: Aim: To experimentally plot the transfer characteristic of NAND gate and to find Δ0 and Δ1 Noise margins.

TEXT BOOK:

LIST OF EXPERIMENTS

1. Measurement of h-parameters
2. Single Stage BJT amplifier
3. Two stage BJT amplifier
4. FET amplifier
5. Differential amplifier
6. Voltage series feedback amplifier
7. Voltage shunt feedback amplifier
8. Current series feedback amplifier
9. Current shunt feedback amplifier
10. RC phase shift oscillator
11. Weinbridge oscillator
12. LC/crystal oscillator.
13. Class B Power amplifier
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**ELECTRONICS & COMMUNICATION ENGINEERING**

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<td>Control System Engineering</td>
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(6+2) 30 Hours
ECONOMICS
UNIT – I


Factors of Production: Meaning and Definition, Characteristics of Land Labour, capital and Entrepreneurship. Division of Labour, Advantages and disadvantages. Formation of Capital. Forms of Business organization; Sole proprietorship, partnership concern, cooperative societies joint stock company. Types of partners, Types of joint Stock companies. Merits and Demerits. (6 periods)

MANAGEMENT

UNIT – II


UNIT – III

Staffing: Meaning and Functions of Personnel Management. Coordination Definition, how to Achieve effective coordination. Controlling; Definition and Process (4 periods)

ACCOUNTANCY

UNIT - IV


Preparation of Final Accounts: Trading Account, Profit and loss Account and Balance Sheet (with simple Adjustments) (7 periods)

REFERENCE BOOKS:
EC 311 COMPUTER ARCHITECTURE

Class: III/IV B.Tech. II Semester
Branch: ECE, EIE
Lectures: 3
University Exam.: 100 marks
Sessionals: 50 marks

Duration of University Examination: 3 hours.

UNIT – I

Introduction: Types of Computers: Analog, Digital and Hybrid. Generation of Computers and their comparison. Dissection of Computer into various blocks; Communication among the blocks; Common bus concept, design of bus lines using MUXs and tristate buffers.

The Arithmetic Logic Unit: General register organization, stack organization of CPU, Instruction formats, Instruction types, addressing modes; Introduction to Assembly Language Programming. BASIC, ALU design: Arithmetic Unit, Logic Unit, and Shift Unit. One stage ALU. Computer Arithmetic: Fixed point arithmetic and floating point arithmetic.

UNIT – II

Control Unit: Instruction sequencing, Instruction interpretation. Control Unit design. Methodologies: Hard wired Control Unit – Illustrative example; Micro programmed control unit; Control Memory, Address Sequencing, Micro Instruction format, Micro program sequencer design, concepts of RISC and CISC.

Memory Unit: Memory hierarchy, Main Memory, RAM, ROM, Memory address mapping; Auxiliary Memory: Magnetic tapes & Discs. Associative Memories: Match logic, Read and Write logics, Cache Memory: Mapping techniques, R/W operations; Virtual Memory: Paging, Segmentation; Interleaved Memories.

UNIT – III

Data Transfer Modes: Synchronous data transfer, Asynchronous data transfer, Strobe Control, Hand Shaking.

I/O Unit: Introduction to peripheral devices. I/O interface, I/O data transfer modes: Programmed I/O; Interrupt Driver I/O; Priority Interrupts; Hardware and Software; DMA controller and Data transfer, I/O Processor – CPU and IOP Communication.

UNIT – IV

8085 CPU: 8085 Architecture, Instruction set addressing modes, Basic assembly language programming, pin configuration, timing diagrams, Interrupts. Basic Assembly Language Programmes – stacks, subroutine, strings.

TEXT BOOK:

REFERENCE BOOKS:
EC 312 ANALOG COMMUNICATION SYSTEMS

Class:III/IV B.Tech. I –Semester Lectures: 3, Tutorial: 1
Branch: ECE University Examination: 100 marks
Duration of University Examination: 3 Hours Sessionals: 50 marks

UNIT-I
Amplitude modulation: Time and frequency domain-description of AM, DSB, SSB & VSB signals-Generation and demodulation AM, DSB, SSB and VSB signals-coherent demodulation-envelop detection-carrier recovery. AM transmitters.

UNIT-II

UNIT-III

UNIT-IV
Noise in Communication System: Sources of Noise, types of Noise – quadrature components of noise – Time domain representation of narrow based noise- signal to noise ratio – Noise figure – Equivalent bandwidth. Noise in AM & FM. Calculation of Signal Power, Noise power. Signal to Noise ratio of SSB, DSB, FM Figure of merit.

TEXT BOOKS:
2. “Principles of Communications” – Taub and Schilling (McGraw Hill)

REFERENCE BOOKS:
2. “Analog Communication Systems” – P.Chakrabarthi (Dhanpatrai & Co.)
UNIT – I

INTRODUCTION: (9+3)
Types of systems, Properties of systems, Linearity, Time-invenience, Stability, Causality. Open loop control system, Closed loop control system, Effect of Feedback on over all gain, Stability and Sensitivity.

MATHEMATICAL MODES OF PHYSICAL SYSTEMS:
Electrical, Mechanical and Electromechanical systems, Transfer function of physical systems by Block diagram reduction techniques and signal flow graphs, Drawing a signal flow graph from a block diagram.

UNIT – II

CONTROL SYSTEM COMPONENTS: (9+3)
AC and DC servomotors, Synchros, Tacho generator and Potentiometer.

TIME DOMAIN ANALYSIS:
Design specifications, Typical test signals, Time response of first order and of 2nd order systems, Time domain specifications, Basic control actions like P, PI, PD, PID and derivative feedback, Steady State error and error constants, Routh Hurwitz Criterion, Concept of root locus and construction of root loci, Effects of adding poles and zeros.

UNIT – III

FREQUENCY DOMAIN ANALYSIS: (9+3)
Frequency response of closed loop systems, Specifications, Correlation between frequency and time domain specifications, Polar plots, Gain Margin and Phase Margin, Bode plots, Nyquist stability criterion, Relative stability using Nyquist stability criterion

UNIT – IV

STATE VARIABLE ANALYSIS OF CONTINUOUS SYSTEMS: (9+3)
Concepts of state, State variables and state model, Derivation of state model from transfer function, Diagonalization, Derivation of transfer function from state model, Solution of state equations, State transition matrix, Concept of Controllability and Observability.

COMPENSATION: Elementary treatment of Compensation.

TEXT BOOKS

REFERENCES
EC 313 PULSE AND DIGITAL CIRCUITS

Class: III/IV B.Tech. I Semester Lectures: 3, Tutorial: 1
Branch: ECE University Examination: 100 marks
Duration of University Examination: 3 hours Sessionals: 50 marks

UNIT – I
WAVE SHAPING CIRCUITS: Clipping and clamping circuits, Differentiator and Integrator circuits, simulation of arbitrary transfer characteristics.

SWEEP CIRCUITS: Linearisation of Sweeps, Bootstrap and miller voltage sweep circuits, Principle of current sweep circuits.

UNIT – II
NEGATIVE RESISTANCE SWITCHING CIRCUITS: Voltage Controlled and current controlled negative resistance circuits, its application to switching (using tunnel diode, and UJT).

MULTIVIBRATORS: Switching characteristics and switching times of BJT’s and FET’s. Astable, Monostable and Bistable multivibrators; Symmetric and Asymmetric triggering and Schmitt trigger.

UNIT-III
BLOCKING OSCILLATOR CIRCUITS: A triggered transistor blocking oscillator (Base timing and emitter timing), Astable transistor blocking oscillator, applications of blocking oscillators.

SAMPLING GATES: Basic Operating Principle of gates, Unidirectional diode sampling gates, Bi-directional sampling gates (Using diodes and transistors).

UNIT-IV
SYNCHRONIZATION AND FREQUENCY DIVISION: Principles of Synchronization, Synchronization of Astable Multivibrator, Monostable relaxation circuits as dividers, stability of relaxation dividers (Phase delay and phase jitter), synchronization of a sweep circuit with symmetrical signals, sine-wave frequency division with a sweep circuit, synchronization of a sinusoidal oscillator with pulses.

TEXT BOOKS:

REFERENCE BOOKS:
1. L. Strauss, “Wave Generation and Shaping”
EC 314 LINEAR INTEGRATED CIRCUITS

Class: III/IV B.Tech. I – Semester
Branch: ECE, E&I, EEE
Duration of University Examination: 3 Hours

Lectures: 3
University Examination: 100 marks
Sessionals: 50 marks

UNIT-I

UNIT-II
Applications of Operational Amplifiers: Summing and difference amplifiers, Integrator and differentiator, current to voltage and voltage to current converters, Instrumentation amplifier, sample and Hold circuit.
Non-Linear Applications: Precision Rectifiers – Half wave and full wave, log and antilog amplifiers.
Comparators and wave form generators: OPAMP comparators, Regenerative (Schmitt Trigger), R.C. phase shift and wiens bridge oscillators, Astable Multivibrator (Square wave generator) and Monostable Multivibrator.

UNIT-III

UNIT-IV
Phase Locked Loops: Voltage controlled oscillator, Basic PLL operation, definitions related to PLL, Monolithic PLL and design considerations, transient response of PLL, typical PLL applications (FSK, AM detectors)
Analog multiplexers, DAC types (R-2R ladder weighted ladder and Inverted ladder), ADCs types (Successive Approximation, Dual-Slop, Flash types).
TEXT BOOKS:

2. Ramakant Gayakwad, Opamp and Linear Integrated Circuits, Pearson Education.

REFERENCE BOOKS:

EC 315 PULSE AND DIGITAL CIRCUITS LAB

Class: III/IV B.Tech. I Semester  
Practicals: 3Hrs.
Branch: E&I,EEE  
Sessionals: 25 Marks
Duration of University Examination: 3 hours  
University Examination: 50 Marks

**LIST OF EXPERIMENTS**

1. Linear Wave Shaping
2. Non-Linear Wave Shaping (Clipping and Clamping Circuits)
3. Boot Strap Sweep Circuits
4. Miller Sweep circuits
5. UJT as Relaxation Oscillator
6. Astable multivibrator
7. Monostable multivibrator
8. Bistable multivibrator
10. Sampling gates.
EC 316 LINEAR INTEGRATED CIRCuits laboratory

Class: III/IV B.Tech. I – Semester
Branch: ECE
Duration of University Examination: 3 Hours

Lectures: 3
University Examination: 50 marks
Sessionals: 25 marks

LIST OF EXPERIMENTS

   (i) Open Loop gain
   (ii) I/P bias and offset currents.
   (iii) I/P offset voltage.
   (iv) Slow Rate and
   (v) CMRR

2. Design of square wave generator for a specified frequency and duty cycle, using Op-Amp IC 741.
3. Design of a sinusoidal oscillator for specified frequency based on wiens bridge using IC 741.
4. Design and testing of precision rectifier.
6. Design and testing of Active
   (i) L.P.F.
   (ii) H.P.F
   (iii) B.P.F. for specified frequency.

7. Design a Astable multivibrator using IC 555 timer for a given frequency.
8. Design a Monostable Multivibrator using IC 555 timer for a specified width period.
9. Design a voltage regulator using IC 723 for a given O/P voltage and Load current.
10. Design and testing of PLL parameters using IC 565.

TEXT BOOKS:

1. Roy Choudary, Shail Jain, Linear Integrated Circuits, New Age International.
2. Ramakanth Gayakwad, Opamp and Linear Integrated Circuits, Prentic Hall of India, New Delhi.
# Scheme of Instruction and Evaluation

## II Semester of III Year of 4-Year B.Tech. Degree Programme

**Electronics & Communication Engineering**

<table>
<thead>
<tr>
<th>Course Number</th>
<th>Course</th>
<th>Lectures</th>
<th>Tutorials</th>
<th>Drawing/Practical</th>
<th>Hours of Instruction per week</th>
<th>Scheme Evaluation</th>
<th>Total Marks</th>
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<td>Open Elective</td>
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<td>-</td>
<td>3 Hrs</td>
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<tr>
<td>EC 322</td>
<td>Antennas &amp; Wave Propagation</td>
<td>4</td>
<td>-</td>
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<td>3 Hrs</td>
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<td>EI 323</td>
<td>Micro Processors &amp; Micro Controllers</td>
<td>3</td>
<td>1</td>
<td>-</td>
<td>3 Hrs</td>
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<td>EC 324</td>
<td>Digital Communication Systems</td>
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<td>1</td>
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<td>EC 325</td>
<td>TV and Radar Engineering</td>
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<td>EC 327</td>
<td>Analog &amp; Digital Communication Systems Lab</td>
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OE 321 Open Elective:
- OE 321-A Operations Research
- OE 321-B Management Information Systems
- OE 321-C Entrepreneurship Development
- OE 321-D Forex Foreign Trade
OE311 (A) OPERATIONS RESEARCH

Course : B.Tech. III/IV  I Semester
Branch : Common to all branches
External Examination: 3 Hours
Internal Examination: 2 Hours

Theory: 3 periods/week
External Evaluation: 100
Internal Evaluation: 50

UNIT-I (9)

UNIT-II (9)

UNIT-III (9)

UNIT-IV (9)
Queuing Theory: Description of Queuing Models and applicability. Birth and Death Processes, Single server models with Poisson input and exponential service. Multiple service queueing models.

SUGGESTED TEXT / REFERENCE BOOKS:
2. Kanthiswaroop, etal, Opertions Research, S.Chand & Sons, New Delhi.
OE 311 (B) MANAGEMENT INFORMATION SYSTEMS

Course: III/IV B.Tech I Semester
Branch: Common to all branches
External Examination: 3 Hours
Internal Examination: 2 Hours

UNIT–I
Management Information Systems (MIS): MIS Concept, Definition, Role and Impact of MIS, MIS and Computer, MIS and Academics, MIS and the User.
Role and Importance of Management: Introduction and Approaches to Management, Functions of Manager, Managers and the Environment, Management as a Control System, Management by Exception, MIS – A Support to the Management.

UNIT–II

UNIT–III


UNIT-IV (9)


SUGGESTED TEXT / REFERENCE BOOKS:


OE 311(C) ENTREPRENEURSHIP DEVELOPMENT

Course: III/IV B.Tech I Semester
Branch: Common to all branches
External Examination: 3 Hours
Internal Examination: 2 Hours
Theory: 3 Periods/week
External Evaluation: 100
Internal Evaluation: 50

UNIT-I
Entrepreneurship definition, Significance of Entrepreneurship. Role of Entrepreneurship in development advantages and limitations characteristics of a person to become an entrepreneur, human factor in Entrepreneurship, Motivation, Leadership qualities and the essential skills of communication etc., Role of women entrepreneurship, Agencies dealing with entrepreneurship and small scale Industries. Case studies of successful entrepreneurs. Identification of a variable business opportunity, Various methods.
Activity: Inputs from DIC, SFC, IIC & Nationalized Banks.

UNIT-II
Activity: Visit to a small scale industry.

UNIT-III
Project planning: Product planning and development process, Definition of a project, Sequential steps in executing the project, principles of layouts, Types of layouts, Factors influencing layouts. choosing an optimum layout suitable to the venture. Tenders, Call for quotations, Purchase orders, Procurement and installation of machinery and equipment, Utilities etc. Fundamentals of Production Management, PPC-Concepts, Functions, Long & short run problems. Marketing Management: Definition, Functions and Segments. Financial Management: Objectives & Functions
Activity: Interaction with Entrepreneurs in the field.

UNIT-IV
Personal and Human resource management: Introduction, Definitions, Importance, Factors effecting Major functions of enterprise management. Selection, recruitment, training, placement, development, performance appraisal systems. Legal issues in Entrepreneurship, Intellectual property rights, Issues in setting up the organization.
Activity: Preparation of project report for variable business venture
SUGGESTED TEXT / REFERENCE BOOKS:


2. David H. Holt, Entrepreneurship New venture creation prentice hall of India.


OE 321 (D) FOREX AND FOREIGN TRADE

Course: III/IV B.Tech. I Semester  Theory: 3 Periods/week
Branch: Common to all Branches
External Examination: 3 Hours  External Evaluation: 100
Internal Examination: 2 Hours  Internal Evaluation: 50

UNIT-I  (9)

UNIT-II  (9)

UNIT-III  (9)

UNIT-IV  (9)

SUGGESTED TEXT / REFERENCE BOOKS:


UNIT – I

ANTENNA FUNDAMENTALS: Basic concepts and Antenna Parameters – Radiation Patterns, Patterns in Principal Planes, Main Lobe and Side Lobes, Beamwidth, Beam Area, Radiation Intensity, Beam Efficiency, Directivity and Gain, Resolution, Aperture Concepts and types – Aperture area and efficiency, Effective height. Antenna Theorems Retarded Potentials, Radiation from Small Dipole, Quarterwave Monopole and Halfwave Dipole – Current Distribution, fields, power radiated, Radiation Resistance, D and Ae.

UNIT – II

ANTENNA ARRAYS: 2-element arrays – different cases, N-element Linear Arrays – Broadside, Endfire arrays Derivation of their characteristics and comparison. Principal of Multiplication of patterns, Binomial Arrays.

NON-RESONANT RADIATORS: Introduction, Traveling wave radiators – basic concepts, V-antennas, Rhombic antennas.

UNIT – III


UNIT – IV


TEXT BOOKS:
1. Antennas, by John D.Kraus and Ronald J.Marhefka, TMH.
2. Electromagnetic Waves and Radiating Systems, by E.C.Jordan and K.G.Balman, PHI.

REFERENCES:
EC / EI 323 MICROPROCESSORS & MICRCONTROLLERS

Class: III/IV B.Tech. II – Semester
Branch: ECE, E&I, EEE
Duration of University Examination: 3 Hours
Lectures: 3
University Examination: 100 marks
Sessionals: 50 marks

UNIT – I
Evolution of Microprocessors, 8085 MPU Architecture,
**8086 Family Architecture:** Organization of 8086 CPU, Concept of Memory Segmentation, Segment registers, physical and logical addressing, Instruction set, Addressing Modes.

UNIT – II
**Assembly Language Programming:** Assembler directives, simple Programming of 8086 Implementation of structures, time delays, strings, procedures, macros, pin configuration, Min/Max modes, timing diagrams.

UNIT – III
**Interfacing with 8086:** ADC, DAC interfacing, Interfacing of switches, Keyboards, LEDs, Stepper motor; CRT interface, interfacing through devices like 8255, 8257 and 8253. Interrupts & Priority interrupt controller 8259.

UNIT – IV
**8051 Microcontroller:** Architecture, Instruction set, addressing modes, Assembly language Programming, timers, I/o Ports, interrupts, serial ports, interfacing with LEDS Switches & Stepper Motor. Real Time Clock.

TEXTBOOKS:

REFERENCE BOOKS:
EC 324 DIGITAL COMMUNICATION SYSTEMS

Class: B.Tech. III/IV – II Semester
Branch: ECE
Duration of Unit Examination : 3 Hours

Lectures: 3 Hours
Tutorials: 1
Univ. Examination: 100 marks
Sessionals: 50 marks

UNIT – I
Sampling theorem, PCM, DPCM, DM, ADM.

UNIT-II

UNIT-III

UNIT-IV
Error Control Coding: Linear Block Codes, Binary cyclic Codes, Convolution Codes and BCH codes.

TEXT BOOKS:

1. Digital and Analog Communications – Sam Shanmugam. (Unit-II) John Wiley.
EC 325 TV and RADAR ENGINEERING

Class: B.Tech. III/IV – II Semester
Branch: ECE
Duration of Unit Examination: 3 Hours

Lectures: 3 Hours
Tutorials: 1
Univ. Examination: 100 marks
Sessionals: 50 marks

UNIT-I
Introduction to TV: Basic Television Systems, Scanning systems, Composite video Signal, Television Standards (Indian)


UNIT- II

TV TRANSMITTERS & RECEIVERS: Block Schematic Diagram – Visual Exciter, Aural Exciter, Duplexer, Block Diagram of Monochrome TV Receiver, RF tuner, Video IF and Sound IF response characteristics, Vertical and Horizontal Synchronization Techniques, Keyed AGC.


UNIT – III

INTRODUCTION TO RADAR: The nature of RADAR, Block Schematic of pulse Radar, Radar Range Equation, Radar frequencies Applications of Radars, Minimum detectable signal Integration of Radar Pulses.

CW and FMCW RADAR: Doppler effect, CW Radar – Block Diagram, applications, FMCW Radar – Block diagram and Characteristics.

UNIT – IV

MTI Radar, Limitations of MTI Radar, Blind Speed.

TRACKING RADAR: Tracking with radar, Sequential Lobing, Concial Scan, Mono Pulse Radar, Low angle tracking, Tracking in range Introduction to Radome, ECM, ECCM.

TEXT BOOKS:

REFERENCE BOOKS:

2. Colour Television and Practice – by S.P. Bali, TMH.
EC 326 DIGITAL SIGNAL PROCESSING

Class: III/IV B.Tech. II–Semester  Lectures: 3
Branch: ECE, E&I, EEE University Examination: 100 marks
Duration of University Examination: 3 Hours  Sessionals: 50 marks

UNIT-I

UNIT-II
Infinite Impulse Response (IIR) Filters: Realizability of Ideal Filter, Introduction to IIR Filters, Methods of converting analog transfer function H(s) to its digital equivalent, Necessity of Filter Approximation, IIR Digital filter design using Butterworth Approximation, IIR Digital Filter Design using Chebyshev approximation, comparison of Butterworth and Chebyshev filters.

UNIT-III

UNIT-IV
DSP Architecture: Introduction to Programmable Digital Signal Processors; MAC, Bus structures and memory access schemes, multiported memory, multiple access memory, VLIW architecture, Pipelining, addressing modes, on-chip peripherals. Architecture of TMS320C5X: Introduction, Bus Structure, Central Arithmetic Logic unit, registers, flags, on-chip memory and peripherals, assembly language instructions.

TEXT BOOKS:

REFERENCE BOOKS:
2. Lyons, Understanding DSP (Pearson Education)
3. Adreas Antonio, Digital filter Analysis and Design (TMH)
LIST OF EXPERIMENTS

ANALOG COMMUNICATION

1) Amplitude modulation & Demodulation

2) Frequency Modulation & Demodulation

3) Balanced Modulator

4) Pulse Amplitude Modulation (PAM) & Demodulation

5) Pulse Width Modulation (PWM) & Demodulation

6) Pulse Position Modulation (PPM) & Demodulation

DIGITAL COMMUNICATION

7) Analog signal sampling and reconstruction.

8) Channel TDM pulse amplitude modulation and demodulation.

9) Pulse Code Modulation & De-Modulation, PCM Tx and Rx

10) Delta modulation and demodulation, linear, CSVD.

11) Digital Carrier modulation schemes. (ASK, BFSK, BPSK)
EI 328 MICROPROCESSORS & MICROCONTROLLERS LAB

Class: III/IV B.Tech. II – Semester
Branch: ECE, E&I, EEE
Practicals: 3
University Examination: 50 marks
Duration of University Examination: 3 Hours
Sessionals: 25 marks

LIST OF EXPERIMENTS

Assembly Language Programming on 8086 Microprocessor

1. Study of 8086 kits
2. Finding Sum, Average, Multiplication.
3. Sorting (a) Ascending (b) Descending.
4. Transfer of bytes from DS to ES
5. Code Conversions (i) BCD to Binary (ii) Binary to BCD (iii) Binary to ASCII
6. String Comparison
7. Generation of time Delays – counters
   Interfacing with 8086
8. Wave form Generation using DAC modules (i) Square wave (ii) Sawtooth (iii) Triangular.
9. Stepper Motor interfacing
10. ADC interfacing
11. LED/LCD interfacing.
12. Traffic Controller
   ALP on 8031/51 Micro Controllers.
13. Study of Micro Controller kits, Assembly Language Programming
14. Multiplication, Division
15. Sorting
16. Code Conversion
17. Time delays – Counters

TEXT BOOKS:

# SCHEME OF INSTRUCTION AND EVALUATION

I SEMESTER OF IV YEAR OF 4-YEAR B.TECH. DEGREE PROGRAMME

**ELECTRONICS & COMMUNICATION ENGINEERING**

<table>
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<th>Course Number</th>
<th>COURSE</th>
<th>Hours of Instruction per week</th>
<th>Scheme Evaluation</th>
<th>Total Marks</th>
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<td>EC 411</td>
<td>Micro wave Engineering</td>
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<td>Optical &amp; Satellite Communication Systems</td>
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<td>EC 413</td>
<td>VLSI Design</td>
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<td>EC 417</td>
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**Professional Elective – I EC:**

(4+2) Hours

- **414A** - Digital Image Processing
- **414B** - Neural Networks and Fuzzy Logic
- **414C** - Industrial Electronics
- **414D** - Adaptive Signal Processing
EC 411 MICROWAVE ENGINEERING

Class: B.Tech. IV/IV – I Semester  Lectures: 4 Hours
Branch: ECE  Sessionals: 50 marks
Duration of Unit Examination: 3 Hours  Univ. Examination: 100 marks

UNIT – I

MICROWAVE TUBES: Introduction to Microwaves, Microwave region and bands, Applications, Limitations & losses of conventional tubes at UHF, Microwave tubes – O type & M type classifications.


Helix Traveling Wave Tubes: Significance & types of Slow Wave structures, TWT – features, Principle of Amplification (qualitative treatment), Suppression of oscillations.

O-type backward wave oscillator (Carcinotron) – Features, Principle of working, voltage tunability.

UNIT – II

M-Type tubes: Microwave cross field tubes(M type): Magnetrons – 8 cavity cylindrical Traveling Wave Magnetron – features, Mechanism of Oscillations, Hull cut-off conditions, PI-mode and its separation, o/p characteristics.


UNIT – III

WAVEGUIDE COMPONENTS: Coupling probes & loops, Waveguide windows, Tuning Screws & Posts, Waveguide phase shifters and attenuators.


Scattering Matrix – Significance, formulation and properties, S-matrix of waveguide Tee junctions, Directional Coupler, Circulator and Isolator.

UNIT – IV

TEXT BOOKS:

1. Microwave Devices and Circuits – by Samuel Y.Liao, PHI.

REFERENCES:

1. Microwave and Radar Engineering – by M.Kulkarni.
EC 412 OPTICAL & SATELLITE COMMUNICATION SYSTEMS

Class: B.Tech. IV/IV – I Semester Lectures: 3 Hours
Branch: ECE Tutorials: 1
Duration of Unit Examination : 3 Hours Univ. Examination: 100 marks

OPTICAL COMMUNICATIONS

UNIT – I
OPTICAL FIBER WAVE GUIDES: Basic Optical Laws, Fiber types, Rays and modes, Step index and graded index fibers, Ray Optics Representation, Mode theory of circular wave guides, wave equation in step index fiber, graded index fiber, fiber materials.
TRANSMISSION CHARACTERISTICS OF OPTICAL FIBERS: Attenuation – Absorptron, Scattering and bending losses in fibers, core and cladding losses, Signal distortion in optical wave guides.
Fiber splicing – splicing techniques optical fiber connectors – connector types.

UNIT – II
OPTICAL SOURCES AND DETECTORS: Light emitting diodes – LED structures.
Semi conductor Laser diode – Laser diode modes and threshold condition.
Photo detector – PIN Photo detector and Avalanche Photodiode.

SATELLITE COMMUNICATION

UNIT – III

UNIT – IV
SATELLITE LINK DESIGN: Basic Transmission Theory, System noise temperature and G/T ratio, Design of down links, Up Link Design, Design of Satellite Links for Specified C/N Introduction to multiple access techniques.

TEXT BOOKS:
2. Fiber Optic Communication – D.C. Agarwal.

REFERENCE BOOKS:
1. Optical Fiber Communication – John M. Senior – PHI.
2. Satellite Communication – Agarwal.
EC 413 VLSI DESIGN

Class: IV/IV B.Tech. I Semester
Lectures: 4
Branch: ECE
University Exam.: 100 marks
Duration of University Examination: 3 hours.
Sessionals: 50 marks

UNIT-I
Review of Micro electronics and introduction to MOS Technology: Introduction to IC technology, MOS Technology and VLSI, Basic MOS transistor, fabrication of NMOS, CMOS and BICOMS Transistors, thermal aspects of processing and production of E-beam marks. 9

UNIT – II
MOS and BIMOS Circuit Design Processors: MOS layers, stick diagrams, design rules and layout 2μm and 1.2 μm CMOS rules, layout diagrams and symbolic diagrams.
Basic Circuit Concepts: Sheet resistance, area capacities of layers, delay unit and choice of layers. 9

UNIT-III
Scaling of MOS Circuits: Scaling models and scaling factors, scaling factors for device parameters and limitations of scaling.
Subsystem Design and Layout: Architectural issues, switch logic, gate logic, examples of structured design clocked sequential circuits and system considerations. 9

UNIT-IV
System Design and Design Methods: Design Strategies, CMOS chip design options, design methods, design capture tools, verification tools and examples.
CMOS Testing: Need for Testing, manufacturing test principles, design strategies for test, chip level test techniques, system level test techniques. 9

TEXT BOOK:

REFERENCE BOOK:
EC 414 A DIGITAL IMAGE PROCESSING

Class: IV/IV B.Tech. II Semester  Lectures: 4,
Branch : ECE  University Examination : 100 marks
Duration of University Examination: 3 hours.  Sessionals: 50 marks

UNIT – I

Introduction: Elements of Digital Image Processing system, Digital Image representation, Image model, Sampling and Quantization, Neighbors of pixel, Connectivity, Distance measures, Arithmetic and Logical operations on images, Basic Transformations such as translation, Scaling, Rotation, Perspective Transformations

Image Transforms: Two dimensional DFT and its properties, Walsh Transform, Hadamard Transform, Discrete Cosine Transform, Haar Transform, Slant Transform, Hotelling (K-L) Transform

UNIT – II

Image Enhancement: Brightness and contrast of an image, Simple intensity transformations – Image negatives, Linear mapping, logarithmic mapping, Gray level thresholding; Image histograms, histogram equalization, histogram specification, local enhancement; spatial filtering: smoothing filters – low pass, Rank filters, Median filters, min-max and range filters; sharpening filters – high pass, high boost and Derivative filters; Enhancement in frequency domain, Generation of spatial masks from frequency domain specification.

UNIT – III

Image Compression: Redundancy – Coding redundancy, interpixel redundancy, Psychovisual redundancy; Root mean square error, Image compression system model, noiseless and noisy coding, error free compression – Huffman coding, Bit-plane coding, constant area coding, lossless predictive coding; Lossy compression – Lossy predictive coding, Transform coding

UNIT – IV

Image Segmentation: Detection of discontinuities – Point detection, line detection, Edge detection, pixel connectivity; Region – Oriented segmentation – Region similarity, Region growing, Limitations of region growing, Region splitting and Merging

Morphological Image Processing: Structuring element, Fitting and hitting, Dilation, Erosion, Opening and closing, Hit–or–Miss Transform, Basic Morphological Algorithms, Grey Scale Morphology

TEXT BOOKS:
2. B.chanda, D.Dutta Majumder, Digital image processing and analysis, Prentice Hall of India, New Delhi.

REFERENCE BOOKS:
UNIT – I

**Biological Neural Networks:** Neuron Physiology, Neuronal Diversity, Specifications of the brain, They Eye’s Neural Network.

**Concepts of Artificial Neural Networks:** Neural Attributes, Modeling, Basic Model of Neuron, Learning in Artificial Neural Networks, Characteristics of ANNs, ANN Parameters, ANN Topologies, ANN adaptability, The stability Plasticity Dilemma.

UNIT – II


UNIT – III

**Fuzzy Logic:** Propositional Logic, The Membership function, Fuzzy logic, Fuzzy Rule Generation, Defuzzification of Fuzzy Logic, Time – Dependent Fuzzy Logic, Crisp logics, Temporal Fuzzy logic (TFL), Time Invariant Membership function, Time-variant Membership function, Intervals, Semilarge Intervals, Interval operators, Temporal Fuzzy logic syntax, Applying Temporal Fuzzy operators, Defuzzification of Temporal Fuzzy logic, Applicability of TFL in communication systems

UNIT – IV

**Fuzzy Neural Networks:** Fuzzy Artificial Neural Network (FANN), Fuzzy Neural Example, Neuro-Fuzzy control, Traditional control, Neural control, Fuzzy control, Fuzzy – Neural control.

**Applications:** Signal Processing, Image Data Processing, Hand written characteristics Recognition, Visual Image Recognition, Communication systems, Call processing, Switching, Traffic control Intelligent control, Optimization techniques.

**TEXT BOOK:**

**REFERENCE BOOKS:**
UNIT – I

Characteristics of Power Devices: Introduction of power semi conductor devices like SCR, DIAC, TRAIC, GTO, MOSFET, UJT, IGBT and their characteristics. Two transistor modes of SCR, protection of SCR against over voltages, over current and voltage and current transients. 

Gate Triggering circuits, Resistance, Resistance – capacitance Trigger circuits, UJT as relaxation oscillator, series and parallel operation of SCRs, String efficiency, Different methods of forced communication Techniques.

UNIT – II

Phase controlled Rectifiers: Phase Angle control Single phase three phase, halfwave, full wave, Half controlled and Fully controlled with and without free wheeling diodes for resistive and inductive loads, effect of source inductance, Dual converters, Power factor improvements.

UNIT – III

Choppers: Basic circuit, step-up step-down, classification of choppers on the basis of various quadrants, chopper commutation, Jones and Morgan chopper.”

Inverters: Series inverter, parallel inverter, voltage source inverters, and current source inverters, 1-phase and 3-Phase bridge inverters.

UNIT – IV

AC Voltage Controllers: Single Phase AC Controllers with R and RL loads, Three Phase AC Voltage Controllers with Star and Delta connected loads.

Cyclo converters: Principle and operation of Single phase to single phase, single phase to 3-phase, 3-phase to 1-phase Cyclo converters.

Industrial Applications: Uninterrupted power supply, Switched mode power supply. Closed loop control of AC & DC drives and its applications.

TEXT BOOK:

REFERENCE BOOKS:
UNIT – I

Multirate Digital Signal Processing: Multirate Signal processing, Decimation, Interpolation, Time domain and frequency domain characterization of sampling rate alteration devices, Fractional sampling rate conversion, Direct-form FIR structures, Polyphase filter structures, Time-variant filter structures, Multistage implementation of sampling rate conversion, Design of Phase shifters, Interfacing of digital system with different sampling rates, Implementation of Narrow band low pass filters, Implementation of digital filter banks, sub band coding of speech signals, Quadrature mirror filters, Transmultiplexers, oversampling ADCs and DACs. 9

UNIT – II

Power Spectrum Estimation: Cross correlation and Auto correlation of discrete – time signals, power spectral density, periodogram, use of DFT in power spectrum estimation, non parametric methods for power spectrum estimation – Bartlett method, Welch method, Blackman & Tukey method; Parametric methods for power spectrum estimation – Autoregressive (AR), Moving average (MA) and Auto regressive – Moving average (ARMA) models, Yule-Walker method, Burg method, Unconstrained least squares method. 9

UNIT – III

Adaptive Signal Processing: Adaptive Systems, Open and closed loop adaptations, General form of adaptive linear combines, performance surface, gradient and minimum mean-square error, input correlation matrix, eigen values and eigen vectors of correlation matrix, Gradient search methods, Simple gradient search algorithm and its solution, learning curve, newton method, Method of Steepest descent; Gradient component estimation – derivative measurement, Variance of gradient estimate, Weight-vector solution, mis adjustment. 9

UNIT – IV


TEXT BOOKS:

REFERENCE BOOKS:


EC 415  E CAD  LAB

Class : IV/IV B.Tech. I-Semester  Practical : 3 hours
Branch: ECE  Univ. Examination : 50 marks
Duration of Univ. Examination : 3 Hours  Sessionals: 25 Marks

LIST OF EXPERIMENTS:

VHDL / Verilog: Design, Simulation, Synthesis, Implementation of

A. Combinational Circuits:
   i) Adders / Sub factors / Parity Generators
   ii) Multiplexers, Encoders, Decoders.

B. Sequential Circuits:
   i) Flip Flops (SR, JK, D,T)
   ii) Counters
      a) Ripple Counters
      b) Synchronous Counters
   iii) Shift Registers.

C. ALU

D. MEMORIES

E. Layout design– Inverter, NAND and NOR (involves DRC, Spice netlist extraction, Spice Simulation, Using tools like LASI, Winspice)
LIST OF EXPERIMENTS:

1. Antenna demonstration.
2. Mode characteristics of reflex klystron
3. Gunn Oscillator characteristics and power measurement.
4. Wavelength and frequency measurements.
5. Measurement of VSWR
10. Serial Data Link and Modem.
### Scheme of Instruction and Evaluation
**II Semester of IV Year of 4-Year B.Tech. Degree Programme**

**Electronics & Communication Engineering**

<table>
<thead>
<tr>
<th>Course No.</th>
<th>Course</th>
<th>Lectures</th>
<th>Tutorials</th>
<th>Drawing/Practical</th>
<th>Duration of Exam</th>
<th>External Evaluation</th>
<th>Sessionals</th>
<th>Max. Marks</th>
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<th>Total Marks</th>
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<tbody>
<tr>
<td>EC 421</td>
<td>Cellular and Mobile Communication</td>
<td>4</td>
<td>-</td>
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<td>3 Hrs</td>
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<tr>
<td>EC422</td>
<td>Data Communication Networks</td>
<td>4</td>
<td>-</td>
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<td>3 Hrs</td>
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<tr>
<td>EC 423</td>
<td>Professional Elective-II</td>
<td>4</td>
<td>-</td>
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<td>3 Hrs</td>
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<tr>
<td>EC 424</td>
<td>DSP Lab</td>
<td>-</td>
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<td>3</td>
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<td>EC 425</td>
<td>Project Work &amp; Seminar</td>
<td>-</td>
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<td>8</td>
<td>Report &amp; Viva</td>
<td>100</td>
<td>150</td>
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<td><strong>TOTAL</strong></td>
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<td>450</td>
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</table>

*(3+1) 23 Hrs.*

**Professional Elective-II:**

- **EC423A** - Embedded System Design
- **EC423B** - Digital System Design
- **EC423C** - Mixed Signal Processing
- **EC423D** - Radar Signal Processing

*During these 6 hours there will be no formal contact between the guide and the student group

* Based on report seminar and Viva -Voice
UNIT-I

Elements of Cellular Radio System Design:
Max. number of Calls per hour per cell, Max. number of frequency Reuse channels, cochannel Interference Reduction factor, Cell Splitting.

UNIT-II
Co-Channel Interference Reduction:
Co-Channel Interference, Exploring Co-Channel interference Areas in a system, Design of an omnidirectional Antenna system (worst case), Design of Directional Antenna System, Reduction of Co-Channel Interference by means of a Notch in the tilted antenna pattern, Power Control.

Types Of Non Co-Channel Interference:
Adjacent Channel Interference, Near-End-Far-End Interference, cross talk, effects on coverage and Interference by power decrease, Antenna Height decrease, Beam tilting, Effects of Cell-Site Components, Interference between systems.

UNIT-III
Frequency Management and Channel Assignment:
Frequency Management, Set-Up Channels, Definition of Channel Assignment, Fixed channel Assignment.

Handoffs and Dropped Calls:
Initiation of a Hand off, Delaying a Handoff, forced Handoffs, Power-Difference Handoffs, Mobile Assisted Hand off (MAHO) and Soft Hand off, Cell-site Handoff only, Intersystem Handoff.

UNIT-IV
Cell Coverage for Signal and Traffic:
Mobile point-to-point model, propagation in Near-in distance, Long distance propagation, cell-site antenna Height and Signal Coverage Cells, mobile-to-mobile propagation.

Digital Cellular Systems: CSMA, CDMA, GSM

TEXT BOOKS:

REFERENCE BOOKS:
EC 422 DATA COMMUNICATION NETWORKS

Class: IV/IV B.Tech. II Semester  Lectures: 4
Branch : ECE  University Examination : 100 marks
Duration of University Examination: 3 hours.  Sessionals: 50 marks

UNIT – I

Introduction: A Communications model, Data Communications, Data Communications Networking, Protocol and Protocol Architecture, Standards.
Data link control: Flow Control, Error Detection, Error Control, High – Level Data Link Control (HDLC), Other Data Link Control Protocols.

UNIT – II

Frame relay: Background, Frame Relay Protocol Architecture, Frame Relay Call Control, User Data Transfer, Network Function, Congestion Control.

UNIT – III

LAN Technology: LAN Architecture, Bus/Tree LANs, Ring LANs, Star LANs, Wireless LANs.
LAN Systems: Ethernet and Fast Ethernet (CSMA/CD), Token Ring and FDDI, 100VG-AnyLAN, ATM LANs, Fiber Channel, Wireless LANs.
Bridges: Bridge Operation, Routing with Bridges, ATM LAN Emulation.

UNIT – IV

Transport Protocols: Transport Services, Protocol Mechanisms, TCP, UDP.

TEXT BOOK:
2. Tannenbaum - Computer Networks
UNIT - I

Introduction to Embedded Systems: An Embedded Systems, Processor in the System, Other Hardware Units, Software Embedded into a System, Exemplary Embedded Systems, Embedded System-On-Chip (SOC) and in VLSI Circuit.

Processor and Memory Organization: Structural Units in a Processor, Processor Selection for an Embedded System, Memory Devices, Memory Selection for an Embedded System, Allocation of Memory to Program Segments and Blocks and Memory Map of a System, Direct Memory Access, Interfacing Processor, Memories and I/O Devices.

UNIT - II


Device Drivers and Interrupts Servicing Mechanism: Device Drivers, Parallel Port Device Drivers in a System, Serial Port Device Drivers in a System, Device Drivers for Internal Programmable Timing Devices, Interrupt Servicing (Handling) Mechanism, Context and the Periods for Context-Switching, Deadline and Interrupt Latency.

UNIT - III


UNIT - IV

Inter-Process Communication and Synchronisation of Processes, Tasks And Threads: Multiple Processes in an Application, Problem of Sharing Data by Multiple Tasks and Routines, Inter Process Communication.

Real Time Operating Systems: Operating System Services, I/O Subsystems, Network Operating Systems, Real-Time and Embedded System Operating Systems, Interrupt Routines in RTOS Environment: Handling of Interrupt Source Call by the RTOS’s,

TEXT BOOK:


REFERENCE BOOKS:


EC 423 (B) DIGITAL SYSTEM DESIGN

Class: B.Tech. IV/IV – II Semester  
Lectures: 4 Hours  
Branch: ECE  
Sessionals: 50 marks  
Duration of Unit Examination : 3 Hours  
Univ. Examination: 100 marks

UNIT - I

Design of Large Scale Digital Systems: ASM Chart Method. Hardware description language and control sequence method, Design using PLAs, PALs, ASICs, PLDs.

UNIT - II

Fault Diagnosis in combinational Circuits: Fault Classes and Models, fault detection and location experiments, Path Sensitization & Boolean difference methods, Kohavi algorithm. Failure Tolerant design, Introduction to Fault-Tolerant VLSI processor arrays.

UNIT - III


UNIT - IV

Programmable Logic arrays: PLA minimization and PLA folding.  
Design for Testability: Faults in PLAs, Test Generation, DFT Schemes, Built in self-test.

TEXT BOOKS:
1. N.N.Biswa: Logic Design Theory (PHI)  

REFERENCE BOOKS:
1. Morris Mano: Digital Design  
2. Lala: Digital system Design using PLGs.  
3. Schaum’s Serries: Digital Design  
EC 423 (C) MIXED SIGNAL DESIGN

Class: B.Tech. IV/IV – II Semester
Branch: ECE
Duration of Unit Examination : 3 Hours

Lectures: 4 Hours
Sessionals: 50 marks
Univ. Examination: 100 marks

UNIT – I
Building blocks for CMOS amplifiers-design of current mirrors, differential amplifiers;

UNIT - II
CMOS operational transconductance amplifiers – Design of signal ended telescopic cascade, folded cascade and two-stage amplifiers; Frequency compensation schemes – Miller compensation. Ahuja compensation and Nested-Miller compensation.
Design of fully deferential amplifiers, discussion of common mode feedback circuits.

UNIT - III
Switched capacitor circuits, design of switched capacitor amplifiers and integrators, Effect of op amp finite gain, bandwidth and offset, circuit techniques for reducing effects of op amp imperfections, switches and charge injection and clock feed-through effects.
Design of sample and holds and comparators.

UNIT – IV
Fundamentals of data converters; Nyquist rate A/D converters (Flash, interpolating, Over sampled A/D and D/A converters.
Design of PLL’s and DLL’s and frequency synthesizers.

Text Books:
1. Analog MOS integrated circuits for Signal processing, R. GREGORIAN AND TEMES.
2. Introduction to CMOS opamps and comparators, R. GREGORIAN.
3. Analog integrated circuits design, D. JOHNS AND K. MARTIN.

Reference Books:
1. Monolithic Phase-locked loops and clock recovery circuits, B. RAZAVI.
UNIT - I
Introduction: Classification of Radars based on functions, principles of operation etc., performance measures and interplay between Radar parameters, Target parameters and Environment parameters.

UNIT - II
Representation of Signals, K-L expansion, Equivalent Low-pass representation of Bandpass signals and noise.

UNIT - III
Range and Doppler Resolution: Ambiguity function and its properties. Local and Global Accuracy. Signal Design. LFM. Polyphase coded signals detection of a Doppler shifted slowly fluctuating point target return in a discrete scatterer environment.

UNIT - IV

TEXT BOOKS:

REFERENCES:
EC 424 DIGITAL SIGNAL PROCESSING LAB

Class : IV/IV B.Tech. II -Semester  
Practicals : 3 hours
Branch: ECE  
Univ. Examination : 50 
marks
Duration of Univ. Examination: 3 Hours  
Sessionals: 25 Marks

LIST OF EXPERIMENTS:

MAT LAB Programming:

i) Representation Signals
ii) Convolution, Correlation, DFT – Calculation.
iii) Filter Design
   a) IIR
   b) FIR

DSP Processor Programming:

i) Convolution, Correlation, DFT calculation.
ii) Filter Design
iii) Applications (Using code composer studio)