## B. Tech. (ECE) VI SEMESTER

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Course Code</th>
<th>Course Title</th>
<th>Scheme of Instruction</th>
<th>Lecture hrs/week</th>
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*(PE-II) Professional Elective–II
PE3204EC: Embedded System Design
PE3205EC: Artificial Neural Networks and Fuzzy Logic
PE3206EC: Adaptive Filter Theory and Applications
PE3207EC: Optical Communication

**(PE-III) Professional Elective–III
PE3208EC: Information theory and Coding
PE3209EC: Wireless Communications
PE3210EC: Radar Engineering
PE3211EC: MOOCs Course

# Please Refer Annexure
UNIT-I

UNIT-II
FIR Filters: FIR digital filter design techniques. Properties of FIR digital filters, design of FIR filters using windows and frequency sampling techniques, linear phase characteristics. Realization diagrams for IIR and FIR filters, finite word length effects.

UNIT-III
IIR Filters: Analog filter design – Butterworth and Chebyshev approximations, IIR digital filter design techniques, impulse invariant technique. Bilinear transform technique. Comparison of FIR and IIR filters, frequency transformations.

UNIT-IV
Multirate signal processing: Introduction, decimation by a factor D, interpolation by a factor I, sampling rate conversion by a rational factor I/D, design of practical sampling rate converter, S/W implementation of sampling rate converter, application of Multirate signal processing.

UNIT-V
DSP Processors: Introduction to Fixed point Digital Signal Processors, TMS 320C54XX processor-architecture, addressing modes, instruction set, Assembly programming, programming issues, Applications of DSP processors.

Suggested Readings:
UNIT – I
Design Abstraction in Digital circuits, Fabrication process flow of nMOS and pMOS transistors, Overview of CMOS and BiCMOS technologies, MOSFET Transistor under static conditions, channel Length Modulation, Velocity Saturation, Sub-threshold Condition, Threshold variations, MOS structure Capacitance, CMOS Latch up, Technology scaling.

UNIT – II

UNIT – III

UNIT – IV
Designing Arithmetic Building Blocks: Adder, Binary Adder, Full Adder, and Mirror Adder, Transmission gate-based Adder, Manchester Carry Chain Adder, Carry Bypass Adder, Carry Look ahead Adder, Carry Save Adder, Multiplier, Carry Save Multiplier, Barrel Shifter, and Logarithmic Shifter. Design of Memory Structures: ROM cells, PROM, EPROM, EEPROM, Flash Memory, SDRAM and DRAM.

UNIT – V

Suggested Readings:

UNIT - I
Circuit switching: Circuit Switching Principles and concepts.
Packet switching: Virtual circuit and Datagram subnets, X.25.

UNIT - II

UNIT - III
Internet Working: The Network Layer in Internet: IPV4, IPV6, Comparison of IPV4 and IPV6, IP Addressing, ATM Networks.

UNIT - IV

UNIT - V

Suggested Reading:
B. Tech. (ECE) VI SEMESTER

PROFESSIONAL ELECTIVE–II

PE3204EC EMBEDDED SYSTEM DESIGN

Credits: 3

Instruction: 3 periods per week
Duration of SEE: 3 hours
CIE: 30 Marks  SEE: 70 Marks

UNIT-I

UNIT-II
ARM Embedded Systems: The RISC design philosophy, The ARM design philosophy, ARM processor fundamentals, registers, current program status register, pipeline, exceptions, interrupts, and vector table, core extensions, architecture revisions, ARM processor families.

UNIT-III
Embedded processing with ARM CORTEX on Zynq: Fundamentals of FPGA, types of FPGA, case study of Xilinx FPGA, Processing System, programmable logic, programmable logic interfaces, security, Zynq 7000 family members, Zynq versus standard FPGA, Zynq versus standard processor.

UNIT-IV

UNIT-V
Introduction to Real Time Operating Systems: Tasks and task states, tasks and Data, Semaphores and shared data. Operating system services: Message queues, mailboxes and pipes, timer functions, events, memory management, Interrupt routines in an RTOS environment.

Suggested Readings:

B. Tech. (ECE) VI SEMESTER

PROFESSIONAL ELECTIVE –II

PE3206EC ARTIFICIAL NEURAL NETWORKS AND FUZZY LOGIC

Credits: 3

Instruction: 3 periods per week     Duration of SEE: 3 hours
CIE: 30 Marks                                                                                 SEE: 70 Marks

Unit –I
Introduction to Neural Networks: Introduction, Biological Neuron, Biological and Artificial Neuron Models, Characteristics of ANN, McCulloch-Pitts Model, Essentials of Artificial Neural Networks: Types of Neuron Activation Function, ANN Architectures, Classification Taxonomy of ANN – Connectivity, Neural Dynamics (Activation and Synaptic), Learning Strategy (Supervised, Unsupervised, Reinforcement), Learning Rules, Applications of ANN.

Unit – II

Unit –III

Unit – IV
Classical & Fuzzy Sets: Introduction to classical sets - properties, Operations and relations; Fuzzy sets, Membership, Uncertainty, Operations, properties, fuzzy relations, cardinalities, membership functions.

Unit - V
Logic System Components: Fuzzification, Membership value assignment, development of rule base and decision-making system, Defuzzification to crisp sets, Defuzzification methods. Fuzzy logic applications

Suggested Readings:
B. Tech. (ECE) VI SEMESTER

PROFESSIONAL ELECTIVE –II

PE3206EC ADAPTIVE FILTER THEORY AND APPLICATIONS

Credits: 3

Instruction: 3 periods per week     Duration of SEE: 3 hours
CIE: 30 Marks                                                                                 SEE: 70 Marks

UNIT - I
Approaches to the development of adaptive filter theory. Introduction to filtering, smoothing and prediction. Wiener filter theory, introduction; Error performance surface; Normal equation; Principle of orthogonality; Minimum mean squared error; example.

UNIT - II
Gradient algorithms; Learning curves; LMS gradient algorithm; LMS stochastic gradient algorithms; convergence of LMS algorithms.

UNIT - III
Applications of adaptive filter to adaptive noise cancelling, Echo cancellation in telephone circuits and adaptive beam forming.

UNIT - IV
Kalman Filter theory; Introduction; recursive minimum mean square estimation for scalar random variables; statement of the kalman filtering problem: the innovations process; Estimation of state using the innovations process; Filtering examples.

UNIT V

Suggested Reading:
UNIVERSITY, WARANGAL-506 009
Department of Electronics & Communication Engineering

B. Tech. (ECE) VI SEMESTER

PROFESSIONAL ELECTIVE –II

PE3207EC OPTICAL COMMUNICATIONS

Credits: 3

Instruction: 3 periods per week     Duration of SEE: 3 hours
CIE: 30 marks         SEE: 70 marks

UNIT -I
Overview of Optical Fiber Communication: Introduction, Historical development, general system, advantages, disadvantages, and applications of optical fiber communication, optical fiber waveguides, basic optical laws, Ray theory, step index and graded index fibers, ray optics representation, fiber materials.

UNIT - II

UNIT - III
Optical Sources and Detectors: Introduction, LED’s, LASER diodes, Photo detectors, Photo detector noise, Response time, double hetero junction structure, Photo diodes, comparison of photo detectors.

UNIT - IV
Fiber Couplers and Connectors: Introduction, fiber alignment and joint loss, fiber splices, fiber connectors and fiber couplers.

UNIT –V
WDM Concepts and Components: WDM concepts, overview of WDM operation principles, WDM standards,

Suggested Reading:
UNIT - I
Coding for Reliable Digital Transmission and storage: Mathematical model of Information, A Logarithmic Measure of Information, Average and Mutual Information and Entropy, Types of Errors, Error Control Strategies. Channel Coding Channel capacity, binary symmetric channel, binary erasure channel, Shannon’s channel coding theorem, Huffman coding.

UNIT - II
Linear Block Codes: Introduction to Linear Block Codes, Syndrome and Error Detection, Minimum Distance of a Block code, Error-Detecting and Error-correcting Capabilities of a Block code, Standard array and Syndrome Decoding, Probability of an undetected error for Linear Codes over a BSC, Hamming Codes. Applications of Block codes for Error control in data storage system

UNIT - III
Cyclic Codes: Description, Generator and Parity-check Matrices, Encoding, Syndrome Computation and Error Detection, Decoding, Cyclic Hamming Codes, shortened cyclic codes, Error-trapping decoding for cyclic codes, Majority logic decoding for cyclic codes.

UNIT - IV
Convolutional Codes: Encoding of Convolutional Codes- Structural and Distance Properties, state, tree, trellis diagrams, maximum likelihood decoding, Sequential decoding, Majority- logic decoding of Convolution codes. Application of Viterbi Decoding and Sequential Decoding, Applications of Convolutional codes in ARQ system.

UNIT - V
BCH Codes: Minimum distance and BCH bounds, Decoding procedure for BCH codes, Syndrome computation and iterative algorithms, Error locations polynomials for single and double error correction.

Suggested Readings:

UNIT-I
Overview of wireless communication system, History of wireless communication, current wireless systems, wireless spectrum, 2G, 3G, 4G and 5G wireless communication standards.

UNIT-II (Qualitative treatment only)
Comparison of digital Modulation schemes: Information Capacity, Bits, Bit Rate, Baud, and M-ARY Coding, ASK, FSK, PSK, QAM, BPSK, QPSK, 8PSK, 16PSK, 8QAM, 16QAM, DPSK, Band Width Efficiency.

UNIT-III
The wireless communication environment, classification of fading channels, different parameters related to fading mechanisms, modeling of wireless systems, system model for narrowband signals, Rayleigh fading wireless channel.

UNIT-IV
Basics mechanism of Code division multiple access (CDMA), fundamentals of CDMA codes, Introduction to MIMO wireless communication systems, MIMO system model, MIMO zero forcing and MMSE receiver.

UNIT-V
Multi carrier modulation, data transmission using multiple carriers, basics of orthogonal frequency division multiplexing (OFDM) systems, cyclic prefix, MIMO-OFDM system

Suggested Readings:
B. Tech. (ECE) VI SEMESTER

PROFESSIONAL ELECTIVE –III

PE3210EC RADAR ENGINEERING

Credits: 3

Instruction: 3 periods per week
CIE: 30 marks
Duration of SEE: 3 hours
SEE: 70 marks

UNIT-I


UNIT-II


UNIT-III


UNIT-IV

Tracking Radar: Tracking with Radar, Sequential Lobing, Conical Scan, Monopulse Tracking Radar –Amplitude Comparison Monopulse (one- and two- coordinates), Phase Comparison Monopulse, Tracking in Range, Acquisition and Scanning Patterns, Comparison of Trackers.

UNIT-V

Suggested Readings:


B. Tech. (ECE) VI SEMESTER

PC3214ECDIGITAL SIGNAL PROCESSING LABORATORY
Credits: 1.5

Instruction: 3 periods per week     Duration of SEE: 3 hours
CIE: 25 Marks                           SEE: 50 Marks

List of Experiments

1. (a) Generation of basic signals based on recursive difference equations.  
   (b) Operations on Basic sequences
2. (a) Linear and Circular Convolutions in time domain and frequency domain  
   (b) Determination of autocorrelation and Power Spectrum of a given signal(s)
3. (a) Fast Fourier Transform – DIT and DIF algorithm  
   (b) Spectrum analysis using DFT
4. (a) Generation of windows – Rectangular, Hamming and Hamming window  
   (b) Design of LPF, HPF, BPF and BSF using windowing technique
5. (a) Design of Butterworth Filter using Impulse Invariant and Bilinear transformation  
   (b) Design of Chebyshev Filter using Impulse Invariant and Bilinear transformation
6. (a) Implementation of Decimation and Interpolation Process.  
   (b) Implementation of I/D sampling rate converters.
7. (a) Study of TMS320C54X DSP processor  
   (b) Arithmetic operation using TMS320C54XX
8. MAC operation using various addressing modes
9. (a) Linear Convolution  
   (b) Circular Convolution
10. (a) FFT Implementation 
    (b) Waveform Generation – Sine wave and Square wave
11. Implementation of FIR filter on DSP processor
12. Implementation of IIR filter on DSP processor

Suggested Readings:

List of Experiments:
Part A (Digital VLSI front-end Design)

1. Develop VERILOG HDL code and Test bench for the following:
   a. Multiplexer, Decoder, Encoder, Parity Generator, D flip-flop, four-bit adder and magnitude comparator using structural modelling
   b. Four-bit parallel adder/subtractor, zero/one detector and JK flip-flop using data flow modelling
   c. Arithmetic and logic unit, D, SR and JK flip-flops with synchronous and asynchronous resets, universal shift register and BCD-seven segment decoder using behavioral modelling
   d. Asynchronous, Synchronous, Ring and Johnson counters.
   e. Sequence Detector using Mealy and Moore type state machines.

2. Develop VERILOG HDL code for eight to three priority encoders using structural modelling and develop a test bench to cover all the functionalities. Assume each gate has a zero delay and three-simulation units delay.

3. Develop VERILOG HDL code for a four-bit carry look-ahead adder in structural modelling. Develop test bench to cover all the functionalities. Assume case (i) zero gate delay and case (ii) inverter: 2 and NAND/NOR gates: 4 simulation units.

4. Develop VERILOG HDL code for four to sixteen decoder using two-to-four decoders and other combinational logic. Develop test bench to cover all the functionalities. Assume case (i) zero gate delay and case (ii) inverter: 2 and NAND/NOR gates: 4 simulation units.

5. Using conditional operator, write Verilog HDL code to shift input data right arithmetic by the number of positions specified by another input shift. Develop test bench to cover all the functionalities.

6. Write Verilog HDL code to realize all bit Zero/One detector. Develop test bench to cover all the functionalities.

7. Develop Verilog HDL code to realize a MOD-10 synchronous decimal up counter with asynchronous reset and clear inputs. Develop test bench to cover all the functionalities.

8. Develop VERILOG HDL code for the state machine of control unit of GCD processor.

9. Develop Verilog HDL code to realize a four-bit universal shift register. Develop test bench to cover all the functionalities.

10. Develop Verilog HDL code to realize a four-bit ring counter with asynchronous reset and clear inputs. Develop test bench to cover all the functionalities.

11. Develop Verilog HDL code to realize a four-bit twisted ring counter with asynchronous reset and clear inputs. Develop test bench to cover all the functionalities.

12. Design a clock generator where its output clk is initialized to 0 and has a period of 500-time units and a duty cycle of 70%.
13. Design four-bit binary to Gray converter and Gray to binary converter.


Part B (Digital VLSI back-end Design)
1. Design and analyze the following CMOS circuits:
   a. Inverter using static, ratioed, dynamic and domino logic styles
   b. Two-input NAND gate
   c. Two-input NOR gate
   d. Two-to-one Multiplexer using transmission gate
   e. Design a one-bit full adder circuit
   f. Design a one-bit SRAM cell.
2. Draw the layout and evaluate the performance of CMOS Inverter and two-input CMOS NAND gate.

Suggested Readings:

Summer Internship is introduced as part of the curricula for encouraging students to work on problems of interest to industries. A batch of two or three students will be attached to a person from an Electronics Industry / R & D Organization / National Laboratory for a period of 8 weeks. This will be during the summer vacation following the completion of the VI semester course. One faculty member will act as an internal guide for each batch to monitor the progress and interacts with the Industry guide.

After the completion of the project, students will submit a brief technical report on the project executed and present the work through a seminar talk to be organized by the department. Award of sessionals are to be based on the performance of the student at the work place to be judged by industry guide and internal guide (25 Marks) followed by presentation before the committee constituted by the department (25 Marks). One faculty member will coordinate the overall activity of Summer Internship.
Annexure

✓ Students should not choose same department subject as an Open elective subject.
✓ Students can select any one of the following subjects as an Open elective subject.

Open Elective subjects offered from different department

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<th>Course Code</th>
<th>Name of the subject</th>
<th>Branch</th>
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<td>OE3213EC</td>
<td>Microprocessor and Interfacing</td>
<td>ECE</td>
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<td>2</td>
<td>OE3207CS</td>
<td>Fundamentals of Data Structures</td>
<td>CSE</td>
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B. Tech. (ECE) VI SEMESTER

OPEN ELECTIVE-I

OE3213EC MICROPROCESSORS AND INTERFACING

Credits: 3

Instruction: 3 periods per week
CIE: 30 Marks

Duration of SEE: 3 hours
SEE: 70 Marks

UNIT I
Evolution of microprocessors, 8085 microprocessor architecture, addressing modes and instruction sets. Basic assembly language programming, pin configuration, timing diagram of read and write operation.

UNIT II
8086 architecture-functional block diagram, register organization, memory segmentation, programming model, pins description in maximum mode and minimum mode, timing diagrams.

UNIT III
Instruction formats, addressing modes, classification of instruction set, assembler directives, macros, 8086 microprocessor assembly language programs: simple programs involving data transfer operation, arithmetic operation, logical operation, branch operation, machine control operation, string manipulations, stack and subroutine operations.

UNIT IV
8255 Programmable peripheral interface block diagram and various modes of operation. Interfacing of ADC, DAC, keyboard, seven segment display, stepper motor interfacing and 8254 (8253) programmable interval timers.

UNIT V
Interrupt structure of 8086, interfacing programmable interrupt controller 8259 and DMA Controller 8257 to 8086 microprocessor. Serial communication standards, RS 232, Serial data transfer schemes and block diagram of 8251 USART.

Suggested Readings:
1. Ramesh Gaonkar, "Microprocessor architecture, programming and applications with the 8085", Penram International Publication (India) Pvt. Ltd.
UNIT-I

Introduction: Introduction to data structure, types of data structures, revision of arrays, memory representation of arrays, operations on arrays, static versus dynamic memory allocation, pointers, self-referential Structure Time complexity.

UNIT-II

Stack-Queue (Linear Data structures): Definition of stack, operations on stack, implementation of stack. Applications of Stack.

UNIT-III

Definition of queue, operations on queue, implementation of queue using arrays Applications of queue, Circular queue and priority queue.

UNIT-IV


UNIT-V

Graph: definition, terminology on graphs, representation of graphs, graph traversal techniques, spanning tree, minimum cost spanning tree algorithms. Applications of Graphs.

Text Books:

References:
ABBREVIATIONS

L : Lectures  
T : Tutorials  
P : Practicals  
CIE : Continuous Internal Evaluation  
SEE : Semester End Examination  
PC : Professional Core  
OE : Open Elective  
PW : Project Work

**Students have to undergo summer internship of 6 Weeks duration at the end of semester VI and valuation will be done in VII semester.**